

148

FINAL TECHNICAL REPORT

PRECISION POINTING CONTROL SYSTEM

13900-6011-R0-01

7 JULY 1971

PPCS ENGINEERING MODEL DESIGN

Contract No. NAS5-21111

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

| | | |
|---|--|------------------|
| Reproduced by NATIONAL TECHNICAL INFORMATION SERVICE U S Department of Commerce Springfield, VA 22151 | | |
| FACILITY FORM 602 | N 71-35769 (ACCESSION NUMBER) | |
| | 212 (PAGES) | G 3 (THRU) |
| | CR-121912 (NASA CR OR TMX OR AD NUMBER) | 21 (CODE) |
| | | 21 (CATEGORY) |

TRW
SYSTEMS GROUP

REPORT 13900-6011-R0-01

FINAL TECHNICAL REPORT

PPCS ENGINEERING MODEL DESIGN

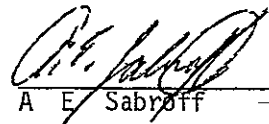
07 JULY 1971

Prepared by R F Gates
A F Haack
G C Hughes
R J Mann
H S Tsou
W Tsusaki
J G Zaremba

Approved by


D K Kirby
Project Manager

Approved by


A E Sabroff
Assistant Manager
Control Systems Laboratory

TRW SYSTEMS GROUP

One Space Park

Redondo Beach, California 90278

CONTRACT NO NAS5-21111

Prepared for

NASA/GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND 20771

Contracting Officer H Arista

Technical Monitor T Huber

ABSTRACT

This report documents the Precision Pointing Control System engineering model design. Detailed layouts with specified internal components are developed for electromechanical, electro-optical, and mechanical equipment. Detailed circuit schematics are developed for electronic equipment.

This report is designed to be used in conjunction with the Final Functional Design and Analysis reports which provide the PPCS system design and related hardware tradeoffs.

TABLE OF CONTENTS

| | <u>PAGE</u> |
|---------------------------------|-------------|
| 1 0 Introduction | 1-1 |
| 2 0 Star Tracker Assembly | 2-1 |
| 2 1 Function | 2-1 |
| 2 2 Configuration | 2-1 |
| 2 3 Operational Description | 2-3 |
| 2 4 Performance Characteristics | 2-4 |
| 2 5 Design | 2-8 |
| 3 0 Sensor Electronics Assembly | 3-1 |
| 3 1 Function | 3-1 |
| 3 2 Configuration | 3-1 |
| 3 3 Operational Description | 3-3 |
| 3 4 Performance Summary | 3-6 |
| 3 5 Design | 3-7 |
| 4 0 Gyro Reference Assembly | 4-1 |
| 4 1 Function | 4-1 |
| 4 2 Configuration | 4-1 |
| 4 3 Operational Description | 4-3 |
| 4 4 Performance Characteristics | 4-4 |
| 4 5 Design | 4-5 |
| 5 0 Reference Block Assembly | 5-1 |
| 5 1 Function | 5-1 |
| 5 2 Configuration | 5-1 |
| 5 3 Operational Description | 5-1 |
| 5 4 Performance Characteristics | 5-1 |
| 5 5 Design | 5-3 |
| 6 0 Attitude Transfer Assembly | 6-1 |
| 6 1 Function | 6-1 |
| 6 2 Configuration | 6-1 |

TABLE OF CONTENTS (Continued)

| | <u>PAGE</u> |
|-----------------------------------|-------------|
| 6 3 Operational Description | 6-2 |
| 6 4 Performance Characteristics | 6-4 |
| 6 5 Design | 6-5 |
| 7 0 Digital Computer Assembly | 7-1 |
| 7 1 Function | 7-1 |
| 7 2 Configuration | 7-1 |
| 7 3 Operational Description | 7-2 |
| 7 4 Performance Characteristics | 7-5 |
| 7 5 Design | 7-6 |
| 8 0 Data Bus | 8-1 |
| 8 1 Function | 8-1 |
| 8 2 Configuration | 8-1 |
| 8 3 Operational Description | 8-2 |
| 8 4 Performance Characteristics | 8-3 |
| 8 5 Design | 8-3 |
| 9 0 Antenna Gimbal Assembly | 9-1 |
| 9 1 Function | 9-1 |
| 9 2 Configuration | 9-1 |
| 9 3 Operational Description | 9-7 |
| 9 4 Performance Characteristics | 9-7 |
| 9 5 Design | 9-8 |
| 10 0 Antenna Electronics Assembly | 10-1 |
| 10 1 Function | 10-1 |
| 10 2 Configuration | 10-1 |
| 10 3 Operational Description | 10-2 |
| 10 4 Performance Characteristics | 10-2 |
| 10 5 Design | 10-2 |
| 11 0 Experiment Gimbal Assembly | 11-1 |

TABLE OF CONTENTS (Continued)

| | <u>PAGE</u> |
|--------------------------------------|-------------|
| 11 1 Function | 11-1 |
| 11 2 Configuration | 11-1 |
| 11 3 Operational Description | 11-4 |
| 11.4 Performance Characteristics | 11-5 |
| 11.5 Design | 11-7 |
| 12 0 Experiment Electronics Assembly | 12-1 |
| 12 1 Function | 12-1 |
| 12 2 Configuration | 12-1 |
| 12 3 Operational Description | 12-2 |
| 12 4 Performance Characteristics | 12-3 |
| 12 5 Design | 12-3 |

REFERENCES

LIST OF ILLUSTRATIONS

| | | <u>PAGE</u> |
|------------|---|-------------|
| FIGURE 1-1 | PPCS Functional Block Diagram | 1-3 |
| 2-1 | PPCS Star Tracker (Engineering Model) | 2-1 |
| 2-2 | SSU Package - Complete | 2-2 |
| 2-3 | SSU Housing and Sun Shade Exploded | 2-2 |
| 2-4 | SSU Telescope - Exploded View | 2-2 |
| 2-5 | Engineering Model Electronics (Test Set-up) | 2-2 |
| 2-6 | STA Optical Schematics | 2-8 |
| 2-7 | Optical Mechanical Telescope Layout | 2-9 |
| 2-8 | Video Processor Block Diagram | 2-11 |
| 2-9 | Voltage Follower | 2-11 |
| 2-10 | Voltage Controlled Attenuator | 2-12 |
| 2-11 | Forward Gain Block | 2-12 |
| 2-12 | Automatic Gain Control Threshold | 2-13 |
| 2-13 | Track Video Threshold Detector | 2-13 |
| 2-14 | Peak Charging AGC Filter | 2-14 |
| 2-15 | Tuned Amplifier | 2-14 |
| 2-16 | Peak Detector | 2-15 |
| 2-17 | Star Presence Threshold Detector | 2-16 |
| 2-18 | Acquisition Scan Generator | 2-17 |
| 2-19 | Track Scan Generator | 2-19 |
| 2-20 | Timing Wave Forms | 2-20 |
| 2-21 | Track Sweep Integrator and Channel Switches | 2-21 |
| 2-22 | Error Detectors | 2-22 |
| 2-23 | Tracking Integrator | 2-23 |
| 2-24 | Coil Drive Amplifier | 2-23 |
| 2-25 | Error Amplifier | 2-24 |
| 2-26 | Video Monostable Multivibrator | 2-25 |
| 2-27 | Acquisition Video Delay | 2-25 |

LIST OF ILLUSTRATIONS (Continued)

| | <u>PAGE</u> |
|--|-------------|
| FIGURE 2-28A Timing for No Acquisition | 2-26 |
| 2-28B Timing for Acquisition | 2-26 |
| 2-29 Mode Flip-Flop Gating Logic | 2-27 |
| 2-30 Plus 12V Regulator | 2-28 |
| 2-31 Minus 12V Regulator | 2-29 |
| 2-32 High Voltage Power Supply and Clock Oscillator | 2-31 |
| 2-33 Bright Object Sensor | 2-32 |
| 2-34 Star Tracker Gimbal Drive | 2-33 |
| 2-35 STA Bearings and Flexure Support | 2-34 |
| 2-36 STA Inductosyn Plates | 2-40 |
| 2-37 STA Data Link | 2-41 |
| 3-1 Circuit Boards Prior to Folding and Mounting | 3-2 |
| 3-2 Assembled Slice | 3-2 |
| 3-3 Slices stacked to form an assembly One row of connectors is for slice-to-slice interconnections Cover for this harness is also shown | 3-2 |
| 3-4 SEA Block Diagram | 3-4 |
| 3-5 SEA Excitation Section | 3-9 |
| 3-6 SEA Preamplifier Pair | 3-11 |
| 3-7 Multispeed Encoder | 3-12 |
| 3-8 SEA Multispeed Encoder | 3-13 |
| 3-9 SEA Single Speed Encoder | 3-17 |
| 3-10 SEA Motor Electronics | 3-19 |
| 3-11 SEA A-D Converter | 3-23 |
| 4-1 Gyro Input Axis Orientation With 6 Gyros | 4-1 |
| 4-2 GRA Block Diagram | 4-2 |
| 4-3 GRA Package | 4-3 |
| 4-4 Gyro Wheel Supply | 4-7 |
| 4-5 Inverter and DC Supply | 4-8 |

LIST OF ILLUSTRATIONS (Continued)

| | | <u>PAGE</u> |
|--------|--|-------------|
| FIGURE | 4-6 AC Amplifier and Demodulator | 4-9 |
| | 4-7 Temperature Controller | 4-10 |
| | 4-8 Rebalance Electronics | 4-11 |
| | 4-9 Voltage-To-Frequency (VFC) Block Diagram | 4-12 |
| | 5-1 Reference Block Assembly Layout | 5-2 |
| | 6-1 Attitude Transfer Optical System Diagram | 6-1 |
| | 6-2 Mechanical System Diagram | 6-3 |
| | 6-3 ATA Functional Block Diagram | 6-4 |
| | 6-4 Autocollimators Cross Section | 6-7 |
| | 6-5 Optics Exploded View | 6-9 |
| | 6-6 ATA Electronics Block Diagram | 6-13 |
| | 6-7 Video Channel Schematic | 6-15 |
| | 6-8 Motor Control Circuits | 6-17 |
| | 6-9 Stepper Motor Control | 6-19 |
| | 6-10 ATA Resolver Circuits | 6-21 |
| | 6-11 ATA Frequency Dividers and Light Source Drivers | 6-23 |
| | 6-12 Resolver Follower | 6-25 |
| | 7-1 DCA/DATA BUS Redundancy Scheme | 7-1 |
| | 7-2 Typical DCA Executive Organization | 7-2 |
| | 7-3 CPU Block Diagram | 7-9 |
| | 7-4 Control Module for Simple Instructions | 7-11 |
| | 7-5 PAU Module Block Diagram | 7-13 |
| | 7-6 OPERAND Arithmetic Module | 7-13 |
| | 7-7 Memory System Block Diagram | 7-15 |
| | 7-8 Memory Bus | 7-16 |
| | 7-9 Input/Output Processor Block Diagram | 7-17 |
| | 8-1 Generalized Data Bus | 8-1 |
| | 8-2 General Organization of the Remote Terminal Unit | 8-4 |

LIST OF ILLUSTRATIONS (Continued)

| | <u>PAGE</u> |
|---|-------------|
| FIGURE 8-3 Standard Mode General Message Format | 8-5 |
| 8-4 RTU Block Diagram | 8-7 |
| 8-5 Logic Schematic, Control I Chip | 8-9 |
| 8-6 Logic Schematic, Control II Chip | 8-11 |
| 8-7 Logic Schematic, Digital Output Chip | 8-13 |
| 8-8 Logic Schematic, Digital Input Chip | 8-15 |
| 9-1 Antenna Gimbal Assembly Interface Drawing | 9-3 |
| 9-2 Antenna Gimbal Assembly Layout | 9-5 |
| 10-1 Antenna Electronics Assembly Block Diagram | 10-3 |
| 10-2 AEA Common Section | 10-5 |
| 10-3 AEA Encoding Electronics | 10-7 |
| 10-4 AEA Motor Electronics | 10-9 |
| 11-1 Earth Pointing EGA Configuration | 11-1 |
| 11-2 Space Pointing EGA Configuration | 11-2 |
| 11-3 EGA Layout | 11-3 |
| 11-4 Method of Latching to Spacecraft During Launch | 11-4 |
| 11-5 Isometric View of Radial Flexure | 11-8 |
| 11-6 Data Link Assembly | 11-11 |
| 11-7 Thermal Control System | 11-13 |
| 12-1 EEA Motor Electronics | 12-5 |

LIST OF TABLES

| | | <u>PAGE</u> |
|-------|--|-------------|
| TABLE | 3-1 Sensor Electronics Assembly - Physical Characteristics | 3-3 |
| | 3-2 SEA Performance Summary . . . | 3-6 |
| | 3-3 Inductosyn Encoding Error Summary | 3-7 |
| | 4-1 Short Term Gyro Random Drift Test Results | 4-5 |
| | 6-1 Performance Characteristics . | 6-5 |
| | 6-2 ATA Bearing Characteristics . . . | 6-6 |
| | 6-3 ATA Resolver Characteristics . | 6-6 |
| | 6-4 ATA Stepper Motor Characteristics | 6-8 |
| | 7-1 DCA Performance Characteristics | 7-5 |
| | 7-2 List of Class I Instructions | 7-7 |
| | 7-3 List of Class II Instructions . | 7-8 |
| | 7-4 CPU LSI Modules . . | 7-14 |
| | 8-1 Data Bus Characteristics | 8-3 |
| | 8-2 RTU Chip Characteristics | 8-8 |
| | 9-1 AGA Drive Unit Parameters | 9-8 |
| | 10-1 Antenna Electronics Physical Characteristics | 10-1 |
| | 12-1 Experiment Electronics Assembly, Physical Characteristics | 12-2 |
| | 12-2 EEA Performance Summary | 12-3 |

1.0 Introduction

The Precision Pointing Control System is an integrated system for precision attitude determination and orientation of gimballed experiment platforms to design goal accuracy of 0.001 degrees (1σ , per axis). PPCS operates in conjunction with a stabilized carrier spacecraft in orbits ranging from low altitude (200 - 2500 nm, sun synchronous) to 24-hour geosynchronous. Functional design, analysis, and simulations of PPCS performance have been documented (Reference 7). The present volume documents the engineering model design of the equipment comprising PPCS.

A summary of PPCS signal interfaces has been extracted from References 4 and included here to aid in understanding the individual equipment design description which follow. For ease of visualization, the functional block diagram shows only two gyro channels (2 of 6), one star tracker (1 of 2), one attitude transfer assembly (1 of 6), and one experiment gimbal and electronics (1 of 6). The elements not shown are assumed identical in all ways to the representative element shown.

2.0 Star Tracker Assembly

2.1 Function

The Star Tracker Assembly (STA) provides a measure of star line-of-sight relative to a coordinate frame defined in the star tracker base. The STA is composed of a two-axis gimbal drive and a null-seeking star sensor. The gimbal is commanded (by the Sensor Electronics Assembly (SEA)) to slew the star sensor to the vicinity of a star. The star sensor provides two axis error signals (optical-electrical boresight relative to star LOS) which are used (by SEA) to point the boresight at the star, obtaining near null operation for the star sensor. The gimbal angle readout combined with the star sensor error signals provide star LOS referenced to the gimbal base.

2.2 Configuration

The STA consists of two separable units, the gimbal and the star sensor. The complete STA is shown in Figure 2-1. This is a picture of the engineering model unit mounted in a test fixture. Cover plates for the wiring were not installed. The gimbal provides a precise, alignable, mechanical mounting for the star sensor and also provides wire wrap-up

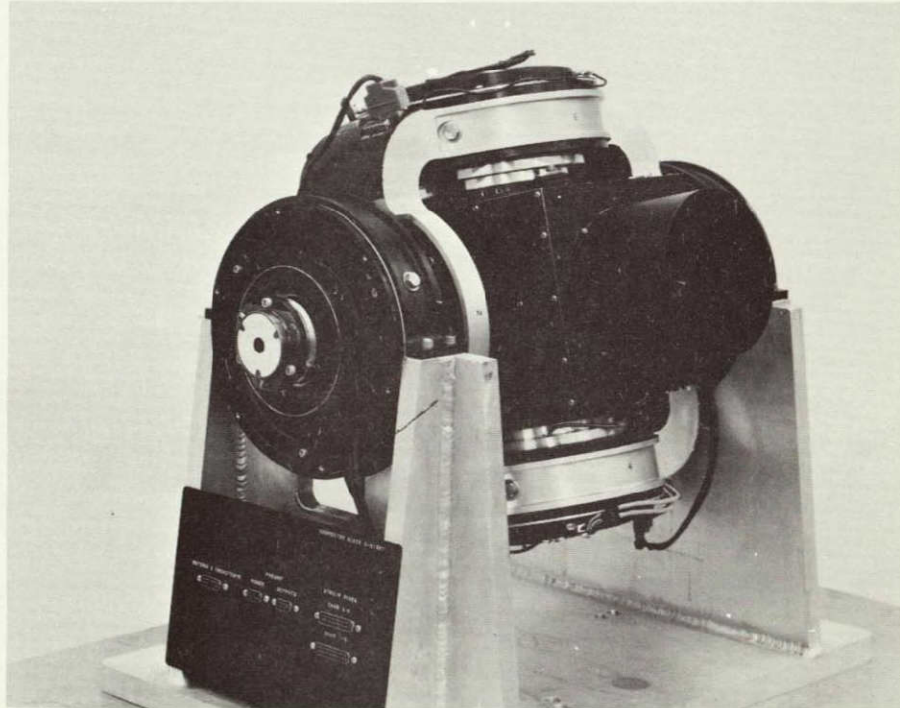


FIGURE 2-1. PPCS Star Tracker (Engineering Model)

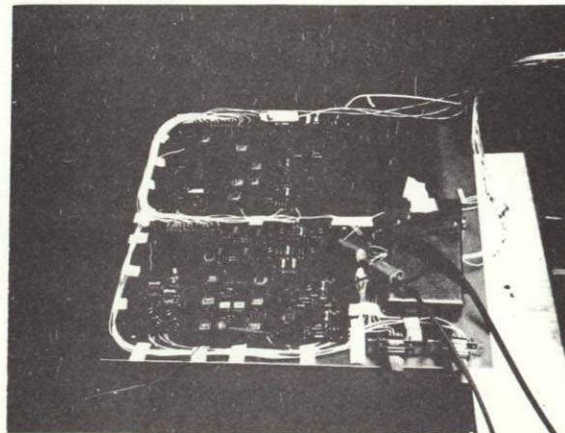
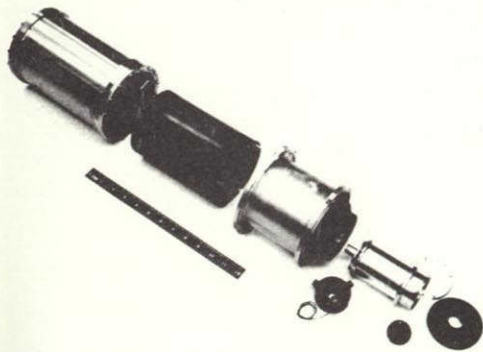
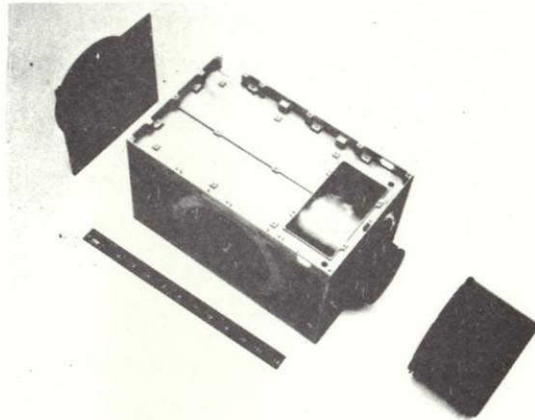


FIGURE 2-4. SSU Telescope - Exploded View

FIGURE 2-5. Engineering Model Electronics (Test Set-Up)

data links to conduct star sensor signals to the outer gimbal interface connector. The gimbal consists of 4 nearly identical drive housings and a structural I-beam ring, which connects the two gimbal axes. Each gimbal housing contains a single-ball bearing, a bearing suspension, a torque motor, two Inductosyn angle encoder plates (or thermal simulators), and a data link. Major portions of the housing and the I-beam are beryllium. Parts of the suspension are titanium alloy. Titanium bolts are used in some locations, and Stellite 6B bearing retainers are used. The bearing balls are tungsten carbide. Preamplifier electronics to amplify the Inductosyn outputs are packaged in the gimbal housings on small, individually shielded PC cards.

The star sensor consists of an aluminum housing and sun shade with aluminum reflective optics, a photomultiplier detector, and integral electronics. The electronics are contained on two large PC cards mounted in the housing (top and bottom), and two other small PC cards mounted at the base of the detector. A high voltage power supply is packaged in a separate can, mounted with one of the large PC cards. A view of the assembled unit is shown in Figure 2-2. The PC cards mount in the housing compartment (top and bottom) as shown in Figure 2-3. Figure 2-4 shows an exploded view of the optics and detector. The electronics (unmounted) are shown in Figure 2-5.

The dimensions of the complete STA are 22" x 16 4" x 17 1" and the total weight is 39 pounds. The mounting of the STA to the spacecraft platform is through 8 mounting holes on the outer drive housings.

2.3 Operational Description

During launch and initial carrier spacecraft orientation, the STA is caged. This is accomplished by driving the two gimbals to the extreme rotational angle ($+ 50^\circ$ outer and $+ 20^\circ$ inner), which brings axial stops to within 0.002" of contact and radial stops into actual contact. A mechanical detent holds the gimbal in this position until initial on-orbit use.

Initial star acquisition is accomplished by applying power to the STA and commanding suitable motor torques (computer commands to the Sensor Electronics Assembly, which appear as properly commutated motor analog voltages at the gimbal) to drive the gimbal so that the star sensor bore-sight is near ($\pm 3^\circ$, two axis) a desired star. Inductosyn gimbal angle readouts are compared to commanded gimbal angles (in the computer) for this operation. The gimbals are then driven in a programmed search pattern covering the $\pm 3^\circ$ uncertainty region while the star sensor scans

its acquisition field-of-view (± 10 arc minutes) with a raster scan (0.25 sec/scan). The gimbal search rate is such that the star sensor scans each area twice. The second scan seeing a star brighter than a fixed lower threshold switches operation automatically to track mode (sensing and mode switch done in the star sensor electronics). In this mode, the sensor scan is reduced to a ± 28 arc sec cruciform pattern.

Upon entering track mode, the star sensor provides error signals relating its boresight to the star LOS. These error signals are used in the Sensor Electronics Assembly to drive the gimbals so as to null the boresight errors. This operating condition is maintained until the computer has obtained a star LOS reading (gimbal angles combined with star sensor error signals). Then a new star is sought by a similar process (with smaller uncertainty). After 5-10 such sightings, the computed attitude will converge to its pre-calibration value and acquisition will be completed.

A phase of calibration followed by normal mode operation will follow.

2.4 Performance Characteristics

2.4.1 Gimbal Unit Performance

| | | |
|--------------------------------------|--------------------|-------|
| Weight | 23 | lbs |
| Power | | |
| Preamps | 1.4 | watts |
| Encoders (and Thermal Simulators) | 16 | watts |
| Motors | 3 | watts |
| Volume (x, y, z) | 22 x 16.36 x 17.12 | |
| Excursion | | |
| Operational | | |
| Inner | ± 15 | deg |
| Outer | ± 45 | deg |
| Caged Condition | | |
| Inner | +20 | deg |
| Outer | +50 | deg |

Bearings

Physical Characteristics

Material

Balls

Tungsten Carbide

Retainers

Stellite 6B

Critical Dimensions

Balls

Roundness

 2×10^{-6} inch

Finish

 1×10^{-6} inch

Retainers

Cone Angle Surface

 20×10^{-6} inch

Offset

 40 ± 4

Stresses

Maximum

Thrust

 130×10^3 lb/in²

Radial

 250×10^3 lb/in²

Nominal

Thrust

 $80 - 100 \times 10^3$ lb/in²

Radial @ 1-g

 170×10^3 lb/in²

Friction Torques

Inner (20 lbs preload)

15.6 in-oz

Outer (35 lbs preload)

28.5 in-oz

Gimbal Structure

Stiffness

Vertical direction

 $0.45 \times 10^6 \frac{\text{lb}}{\text{in}}$

Horizontal direction

 $90 \times 10^3 \frac{\text{lb}}{\text{in}}$

1-g Field Droops

Lateral Orientation

 360×10^{-6} in

Vertical Orientation

 70×10^{-6} in

Stresses

Bending (load vertical)

 $700 \frac{\text{lb}}{\text{in}^2}$

Bending (load horizontal)

 $7200 \frac{\text{lb}}{\text{in}^2}$

Gimbal Alignment Errors

| | Pitch arc sec (3 σ) | Roll arc sec (3 σ) |
|---|--------------------------------|-------------------------------|
| Manufacturing Tolerance | | |
| Run-out | 0 46 | 0 15 |
| Perpendicularity | 0 22 | 0 11 |
| Capability to Align (instrumental limitation) | | |
| Run-out | 1 5 | 1 5 |
| Perpendicularity | 1 5 | 1 5 |
| Stress Relaxation | 0 5 | 0 5 |
| Thermal | | |
| Entire gimbal shifts about z axes | 0 07 arc sec | |
| Entire gimbal shifts about y axes | 0 60 arc sec | |

Gimbal Alignment Sensitivities

| | |
|------------------|--|
| Run-out | 2,000 $\frac{\text{arc sec}}{\text{arc sec}}$ |
| Perpendicularity | 13,000 $\frac{\text{arc sec}}{\text{arc sec}}$ |

Natural Frequency

| | |
|---------------------------|----------|
| System not Caged | |
| x Direction (along roll) | 53 cps |
| y Direction (along pitch) | 53 cps |
| z Direction (along yaw) | 250 cps |
| System Caged | |
| x Direction (along roll) | 320 cps |
| y Direction (along pitch) | 320 cps |
| z Direction (along yaw) | 1100 cps |

Gimbal Drive Motor (each)

| | |
|--|----------------|
| Continuous torque capability @ 18 volts | 60 oz-in |
| Max torque | 1 2 ft-lb |
| Torque ripple | <3 in-oz |
| Power @ 60 oz-in | 6 watts |
| Nominal power | 1 5 watts |
| Residual torque | 2 oz-in |
| Magnetic leakage | 3 gauss @ 1 in |

Inductosyn Encoder

| | <u>Fine Pattern</u> | <u>Coarse Pattern</u> |
|----------|---------------------|-----------------------|
| Accuracy | $\pm 1 6$ sec | ± 14 min |
| Speed | 360 | 1 |
| Power | 2 watts | 2 watts |

Data Link Assembly

Number of conductors

Inner gimbal 88

Outer gimbal 88

Restraint torque 1 in-oz

Current capability per conductor 2 amps

2 4 2 Star Sensor Unit Performance

Detector F4004PMT

Field of View

Acquisition 10 arc min x 10 arc min

Instantaneous 28 arc sec

Optics Folded Gregorian

Tracking Band Width 25Hz

Sensitivity + 3.5 M Ao STAR

Nearest Sun Angle 45°

Tracking Accuracy

Noise Equivalent Angle (+ 3.5 M Star) 0.35 arc sec (1 σ)Electronic Bias Errors 0.18 arc sec (1 σ)Thermomechanical Stability 0.4 arc sec (1 σ)

Error Voltage Outputs

Scale Factor 20 mv/arc sec

Linear Region ± 5 arc minLinearity $\pm 5\%$ Output z into (OK ohms) ≤ 100 ohms

Power Inputs 3 watts

Output Signals

x and y analog errors

Star presence - discrete

Mode - discrete

Star brightness - analog

Bright object presence
- discreteTemperature Range + 20°C \pm 15°C

Size 7 x 7 x 17 in

Weight 16 lbs

2.5 Design2.5.1 Optical System

The optical system is basically a modified or folded Gregorian telescope. Figure 2-6 shows the optical schematic. The primary mirror is a paraboloid with a radius of curvature of 24 828 inches. The secondary mirror is flat, while the tertiary mirror is spherical with a radius of 1 9333 inches.

The diameter of the primary mirror is 4.5 inches, with the secondary mirror and tube assembly providing a central obscuration with a diameter of 3.1 inches. This provides a total collecting aperture of 8.37 sq in.

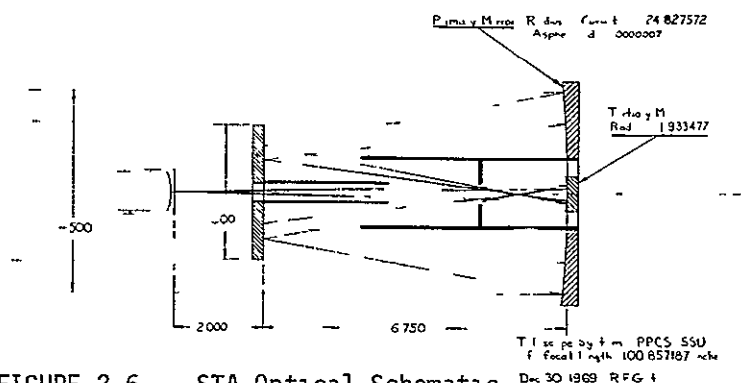


FIGURE 2-6 STA Optical Schematic

All parts of the optical system are reflective, thus there are no chromatic aberrations present. Also, all parts are fabricated from aluminum, which provides a very stable optical system over large temperature extremes.

Summary optical characteristics are listed below:

| | |
|-------------------------|----------------------------|
| Type | Folded Gregorian telescope |
| Equivalent focal length | 2.54 meters |
| Clear aperture | 54 cm ² |
| Equivalent F No | 30.6 |
| Spot size | 0.13 millimeters |
| Primary | |
| Material | Aluminum |
| Curve | Paraboloid |
| Radius of curvature | 63 cm |
| Diameter | 11.43 cm |
| Surface quality | 1/4 wave |

Tertiary

| | |
|---------------------|-------------|
| Material | Aluminum |
| Curve | Spheriodian |
| Radius of curvature | 63 cm |
| Diameter | 11 43 cm |
| Surface quality | 1/4 wave |

Secondary

| | |
|-----------------|------------|
| Material | Aluminum |
| Curve | Flat |
| Diameter | 3 1 inches |
| Surface quality | 1/4 wave |

| | |
|-------------------------|--|
| Surfaces | Polished electroless nickel, evaporated aluminum, with SiO overcoat |
| Useful angle to the sun | 45° |

Sun Shade

The sun shade is designed to allow operation within 45° of the sun. The majority of the sun shade is provided by the general configuration of the housing as shown in Figure 2-7. A relatively short addition is required to prevent any direct sun rays from striking any surface which can be seen by the primary mirror. Adequate baffling is provided throughout the optical path to maximize the number of bounces required for a sun ray to reach the optical surfaces. All interior elements are either black anodized or black oxidized to reduce the percentage of reflection on each bounce.

As shown in Figure 2-7, a rotary solenoid with a shutter is provided so that if the sun comes within the field of view of the sensor, the photocathode of the detector is protected.

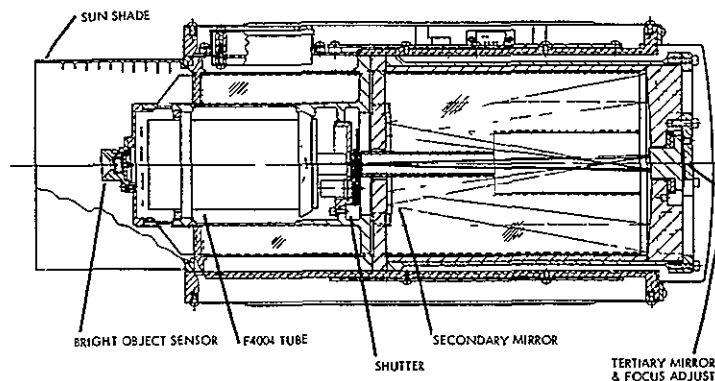


FIGURE 2-7 Optical Mechanical Telescope Layout

2 5 2 Detector

The detector used in the star sensor is a scanning multiplier phototube or image dissector, type F 4004, manufactured by ITT. It has a red-extended S-20 photocathode, providing more sensitivity on cooler stars. The limiting aperture in the tube is circular with a 10 mil diameter, providing an instantaneous photocathode diameter, IPD, of 0.014 inches. When projected out through the optic system, this IPD represents an instantaneous field of view of 28 arc seconds. Sixteen stages of secondary emission multiplication provide an essentially noise free gain of 10^6 to 10^7 . The deflection coils are wound on a machined delvin form which provides the mechanical positioning for the tube in its shield. A triple layer Co-Netic magnetic shield provides the support for the tube and its associated electronics. The deflection coil, tube, and divider network are potted with RTV-11 within the shield. Summary characteristics are listed below.

Image Dissector

| | |
|-----------------|-------------------|
| Type | F4004 |
| Manufacturer | ITT |
| Photocathode | S-20 Red extended |
| Peak response | 0.7 amperes/watt |
| Multiplier gain | 10^7 |
| Noise | Neg |
| Voltage | -1800 volts |
| Bleeder current | 60 μ a |

Shield

| | |
|--------------|-----------------|
| Material | Co-netic A-A |
| Manufacturer | Perfection Mica |
| Thickness | 0.51 mm |
| Layers | 3 |
| Attenuation | >1000 l |

2 5 3 Star Sensor ElectronicsVideo Processor

The function of the video processor is to amplify and selectively shape the image dissector signal outputs. During the star sensor acquisition mode, automatic gain control and threshold circuits select only the largest amplitude video signals and trigger mode logic circuits. When the star sensor is in the track mode of operation, the tube signal is amplified and threshold detected to provide a pulsewidth modulated logic signal to the star sensor error detector.

Another section of the video processor containing a tuned filter develops an analog voltage proportional to the peak output amplitude of the detector and a discrete logic level indicative of star presence whenever the signal level exceeds a fixed reference value

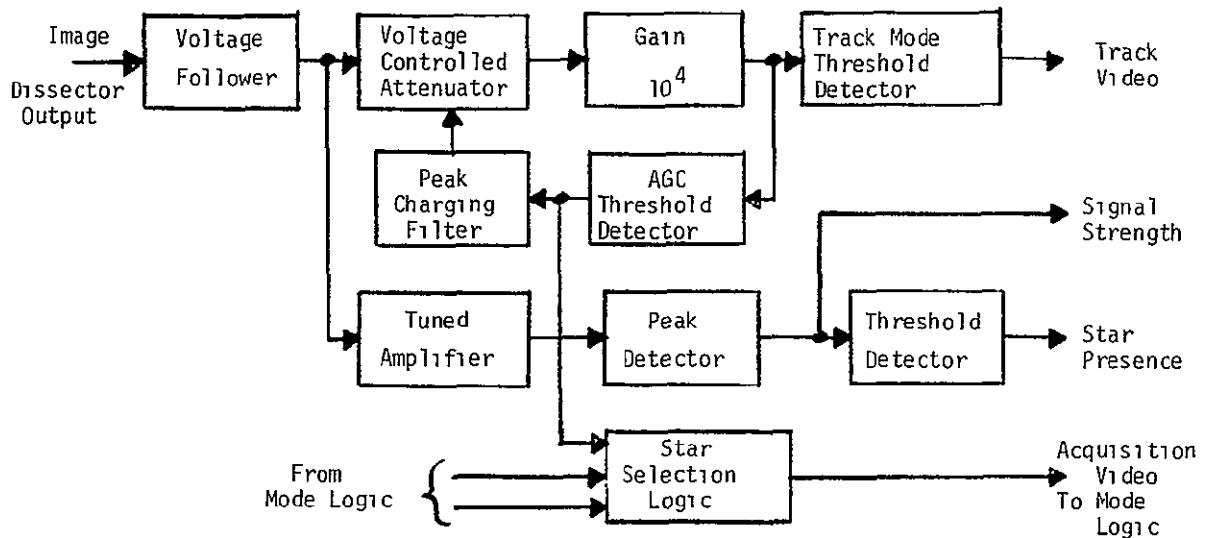


FIGURE 2-8 Video Processor Block Diagram

Input Voltage Follower

The image dissector behaves as a constant current source and is terminated in a 150K load resistance. The input voltage follower is then used to provide a low output impedance to the next stage. The high frequency bandwidth of the video processor is established in this stage by shunting the tube load resistor with an 100pf capacitor since upper bandwidth control must be established outside the automatic gain control loop. The bandwidth is set to 10.6 Kc.

The voltage follower is a LM102 integrated circuit located in the tube assembly.

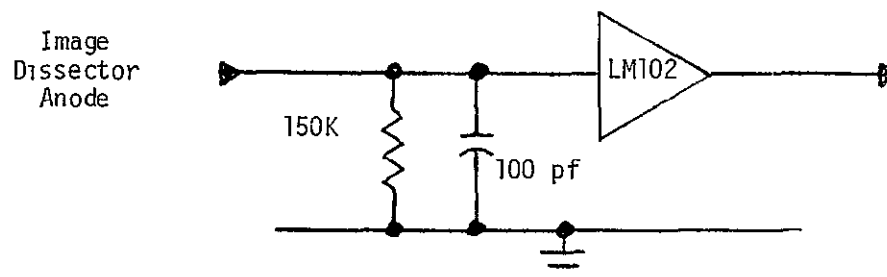


FIGURE 2-9 Voltage Follower

Voltage Controlled Attenuator

The gain control element is a field effect transistor connected in parallel with a 20K resistor. The maximum attenuator gain when the FET is off is 0.5 and the minimum gain with the FET full on is 3×10^{-3} . Thus, the gain control range is 167.

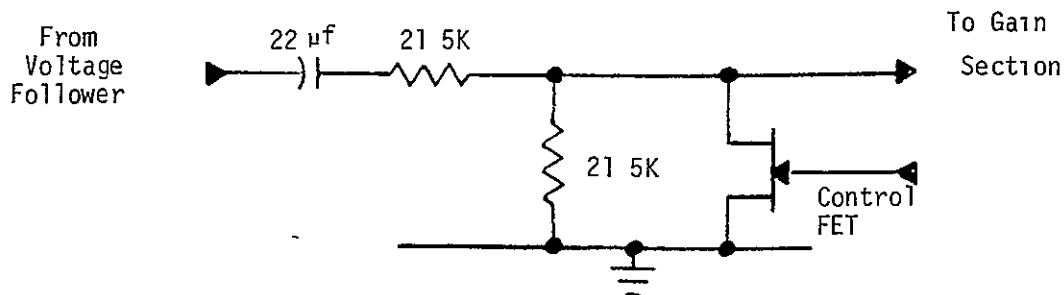


FIGURE 2-10 Voltage Controlled Attenuator

Forward Gain Block

The attenuator circuit is followed by a constant gain block consisting of two LM101 operational amplifiers. The nominal total gain is 400.

To avoid dc offset voltages, each stage is ac coupled.

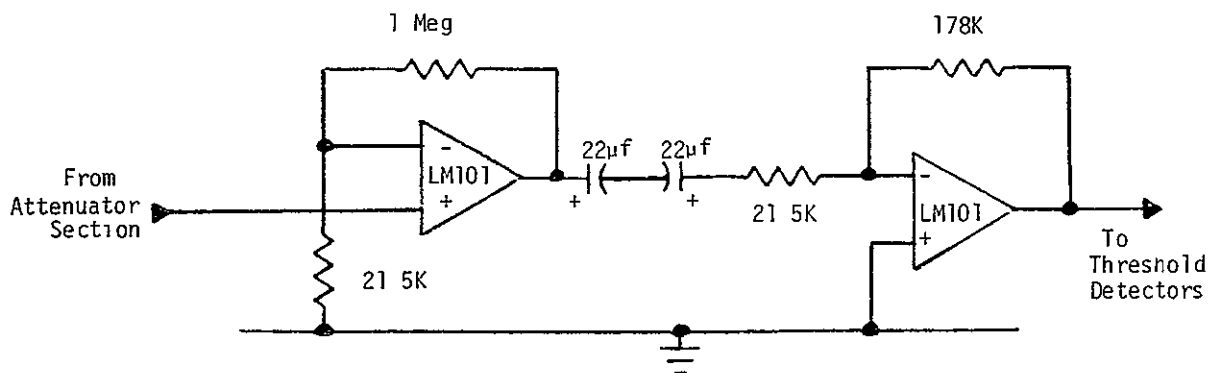


FIGURE 2-11 Forward Gain Block

Automatic Gain Control Threshold Detector

An LM101 operational amplifier is operated open loop as the AGC threshold detector. The amplifier negative input is set to a reference value of approximately 6 volts by a resistive divider from the +12 volt supply. The positive input is capacitively coupled to the gain block output.

The threshold detector output is at its most negative extreme until the amplified video exceeds the 6 volt reference level at which time a positive voltage pulse occurs.

The detector negative output is clamped at -5 volts by a IN752A zener diode connected to pin 8 of the LM101. A IN3604 diode in series with the zener prevents breakdown in the forward direction. The positive pulses are of an amplitude almost equal to the plus supply voltage.

Since the signal voltage to the threshold detector is ac coupled, the AGC loop will limit the signal to a peak value of 6 volts on the very low duty cycle acquisition video and will limit the signal to 12 volts peak to peak during the track mode when a 50% duty cycle sinusoidal type signal is present.

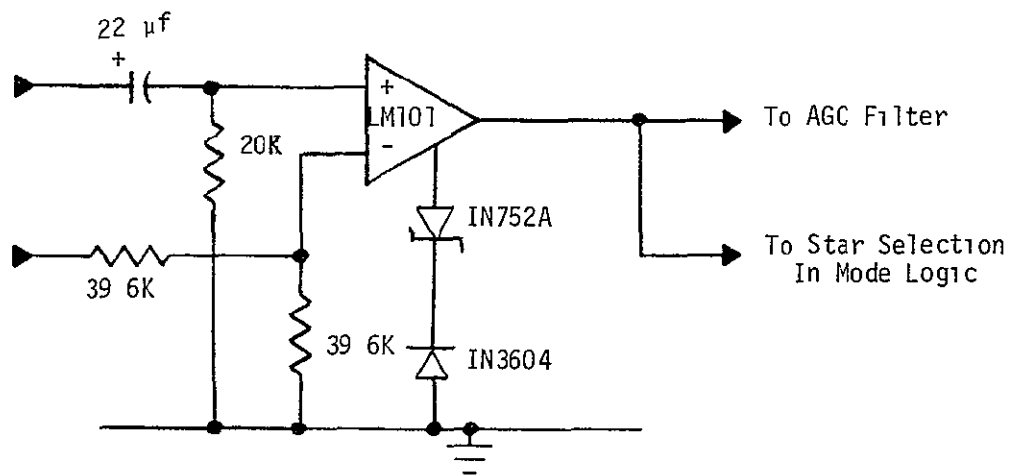


FIGURE 2-12 Automatic Gain Control Threshold

Track Video Threshold Detector

The AGC controlled video signal output of the gain block is also capacitively coupled to an LM101 used as a zero crossing detector to provide the 0 to +5 discrete logic signal called track video.

The LM101 is operated open loop with the output clamped to +5 volts and zero volts by a zener diode connected to pin 8 of the LM101.

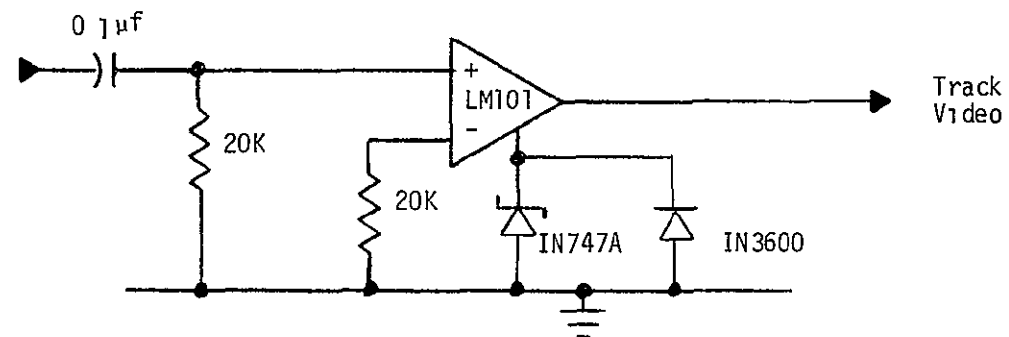


FIGURE 2-13 Track Video Threshold Detector

Peak Charging AGC Filter

The AGC threshold detector drives a peak charging RC filter which sets the control voltage on the gain control field effect transistor. This filter has a short charge time constant (15 ms) and a long discharge time constant (15 seconds) with their ratio being 1000.

The charge time constant determines how much the gain is reduced due to a video pulse exceeding the threshold and the discharge time constant determines how rapidly the gain recovers or increases in the absence of video.

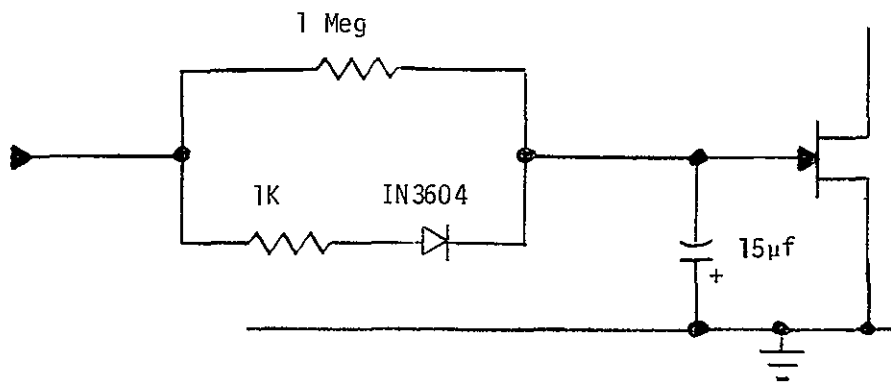


FIGURE 2-14 Peak Charging AGC Filter

Tuned Star Signal Amplifier

The tube assembly voltage follower output is also ac coupled to a tuned bandpass amplifier having a peak gain of approximately 14 and a Q of 12. The circuit is tuned to the 1200 Hz fundamental component of the track mode video.

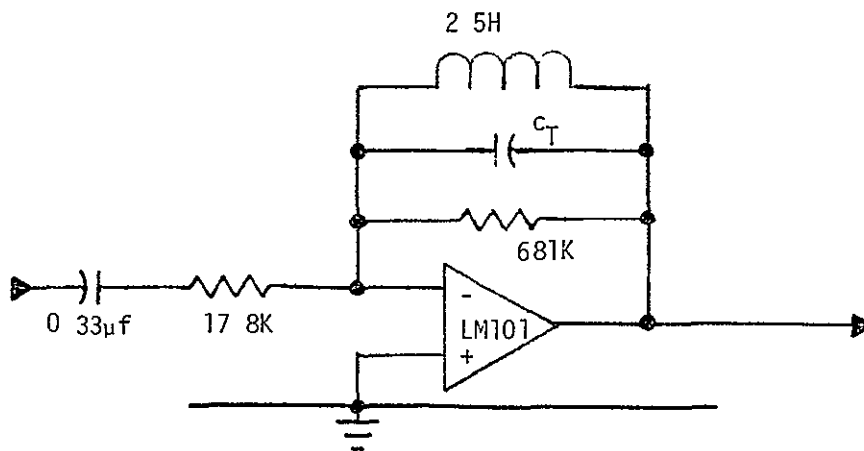


FIGURE 2-15 Tuned Amplifier

Peak Detector Stage

The tuned amplifier output is positive peak detected to develop a dc voltage proportional to the peak tube video. The peak detection is performed with an LM101 operational amplifier, a IN3600 diode and a charging capacitor. The dc feedback around the operational amplifier, also provides additional gain in addition to the peak detection function. The peak detected output is fed to two separate RC filters. The basic output of the SSU is a RC filter which attenuates the peak detected signal by a factor of 0.67.

The other filter, with a 2 millisecond time constant, is ac coupled to the star presence threshold detector.

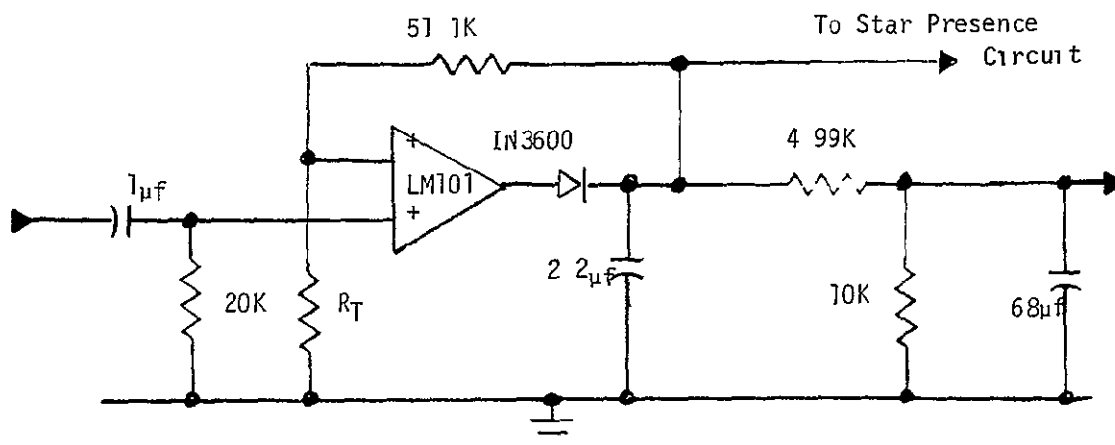


FIGURE 2-16 Peak Detector

Star Presence Threshold Detector

The star presence threshold detector is an LM101 operational amplifier with the signal strength voltage fed to the non-inverting input and a fixed positive reference voltage connected to the inverting input. A zener diode clamp on pin 8 of the LM101 sets the correct output logic level.

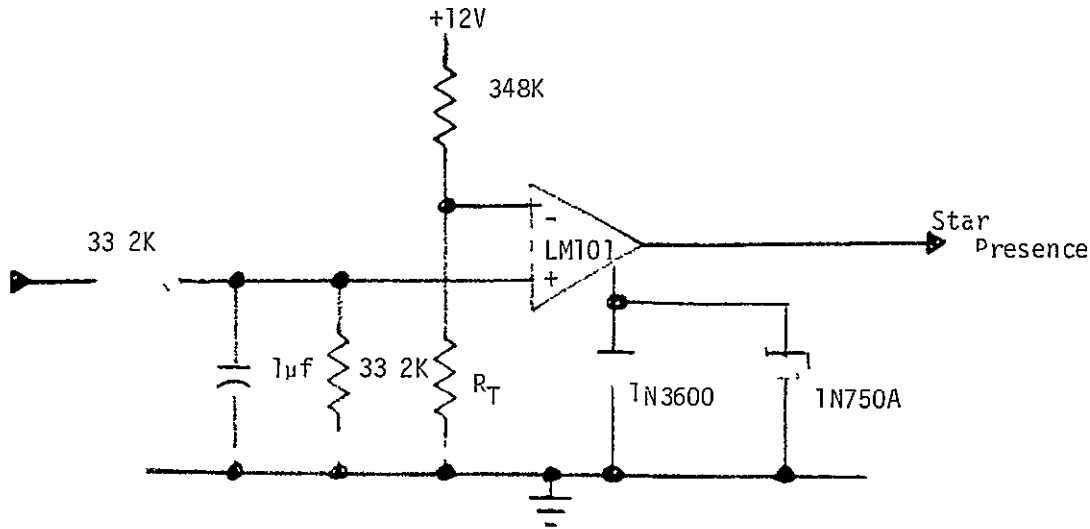


FIGURE 2-17 Star Presence Threshold Detector

Acquisition Video Gate

The output of the acquisition threshold is coupled to a NAND gate which blanks out any video signals occurring during the acquisition scan line retrace. The NAND gate which blanks out any video signals occurring during the acquisition scan line retrace. The NAND gate output is used to trigger a 15 millisecond MSMV in the mode logic.

Acquisition Scan Generator

When the SSU is in the acquisition, or search, mode of operation, a 32 by 32 step digital scan of a 10 minute square field of view is made.

The acquisition scan is generated by two 5 bit D/A converters whose outputs are fed to the deflection coil drivers.

In developing the sweep drive voltage, a 4800 Hz clock is gated into a 10 bit binary ripple counter made up of integrated circuit JK flip-flops.

The first 5 stages of the counter are then connected to the D/A converter to generate 32 step line scan. The last 5 stages of the counter drive a D/A converter to generate 32 line scans per frame.

With the 4800 Hz clock the frame scan time is 0.213 seconds.

The D/A converters are made up of three Sprague I C flat packs with the output being from an R-2R resistive ladder network.

Upon switchover to the track mode of operation, the 4800 clock input is blocked and the acquisition sweeps remain at the switchover values.

The small amplitude triangular modulation dither used during the tracking mode is developed by the track scan generator

As is shown in Figure 2-19, the basic timing waveforms are developed by a 3 stage binary counter

The last counter switches at a 300 Hz rate and is used to multiplex operation between the X and Y axis

The 600 Hz flip-flop output is used to gate demodulator switching as is discussed in another section.

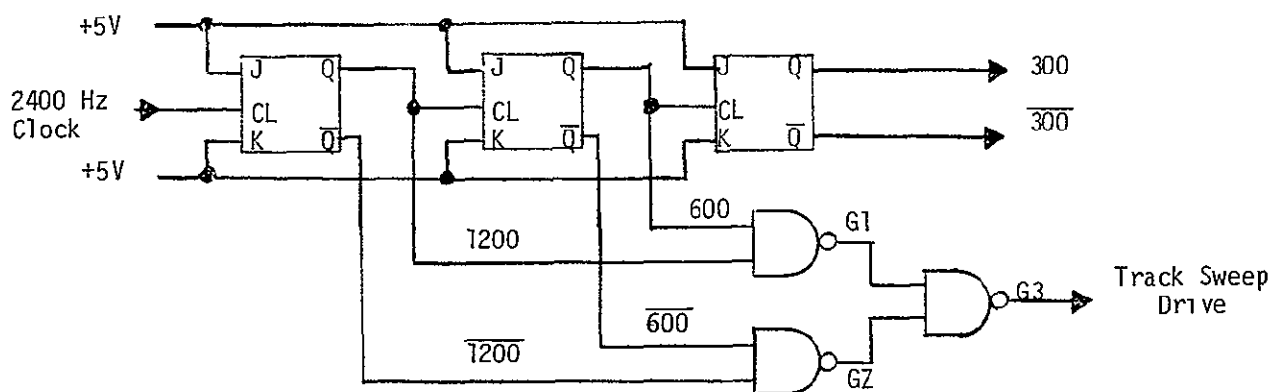


FIGURE 2-19 Track Scan Generator

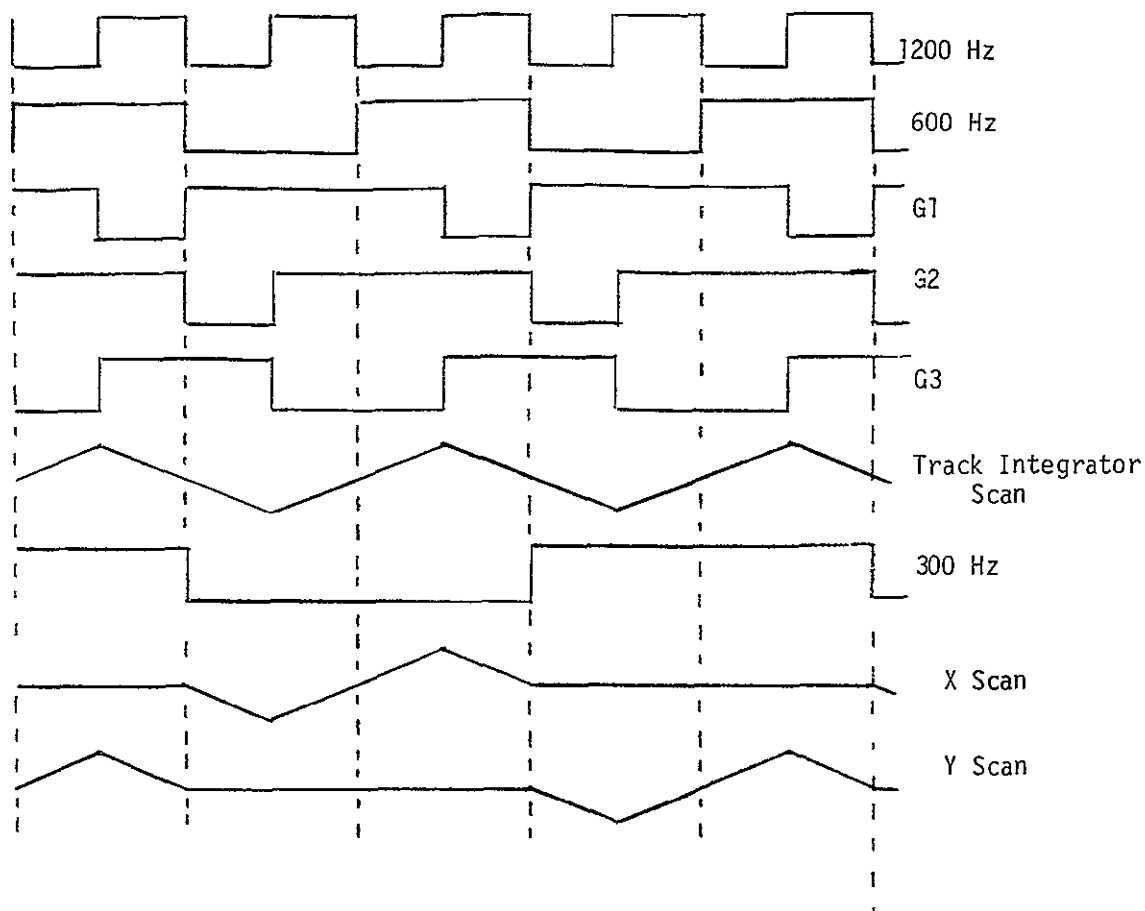


FIGURE 2-20 Timing Wave-Forms

The 1200 Hz and 600 Hz outputs are combined in logic gating to develop a 600 Hz square wave 90 degrees out of phase with respect to the 600 Hz flip-flop output

The 90° phase shifted square wave drives a sweep integrator stage which is an I C operational amplifier with a capacitive feedback

The integrator output is ac coupled to two FET analog switches which are alternately gated on and off by the outputs of 300 Hz timing flip-flop

These outputs are then dc coupled to the X and Y channel coil drivers

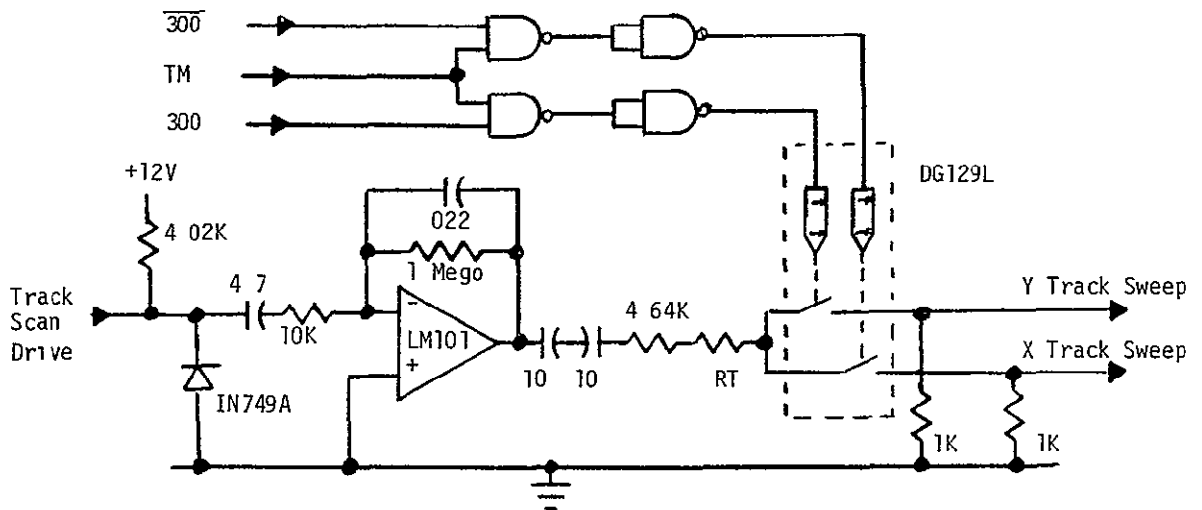


FIGURE 2-21 Track Sweep Integrator and Channel Switches

Tracking Loop Circuits

The tracking loop circuits consist of the error detector, the tracking integrator and the coil drive amplifiers

Error Detector

The error detectors consist of a set of 4 input NAND gates which time separate the track video logic signal into the X and Y channels and into video occurring during the positive track scan and during the negative track scan

The time separated video pulses are then used to switch a reference zener diode voltage into a resistor summing network. The resulting integrator input is a serial train of positive and negative pulses whose average dc value represents the error detector output.

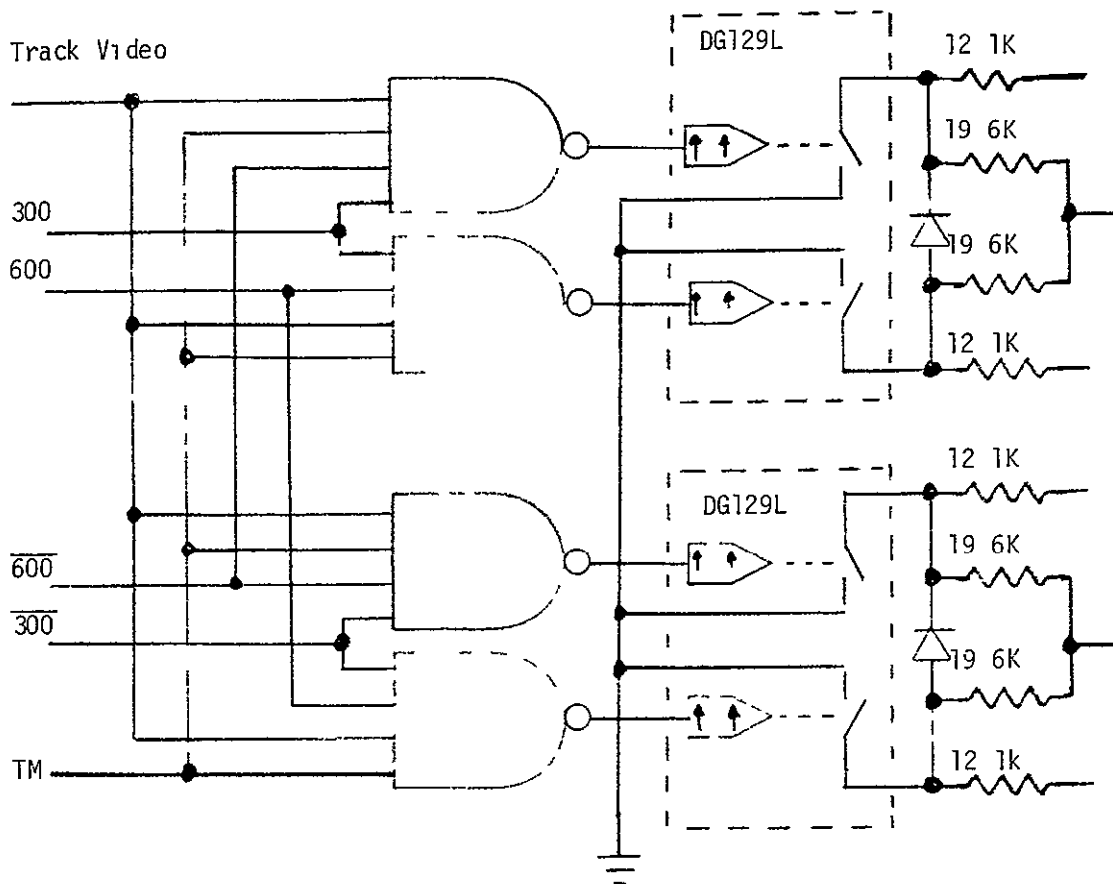


FIGURE 2-22 Error Detectors

Tracking Integrator

The tracking loop integrator is an operational amplifier with capacitive feedback. The input is the resistive summing network of the error detector.

The integrator first order transfer function is K/Z where $K = 13.7$ volts/volt second.

A FET analog switch shunts the feedback capacitor during the acquisition mode and holds the integrator output to zero until tracking starts.

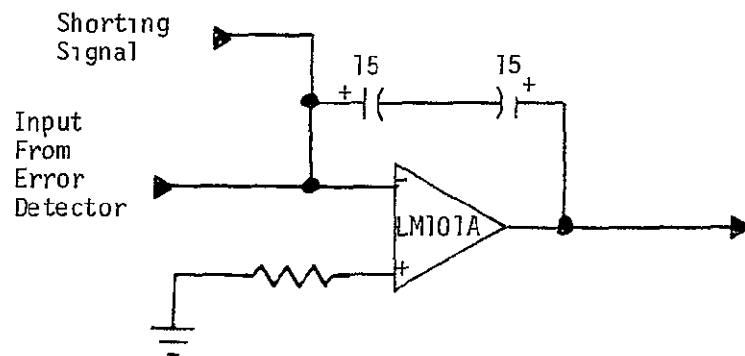


FIGURE 2-23 Tracking Integrator

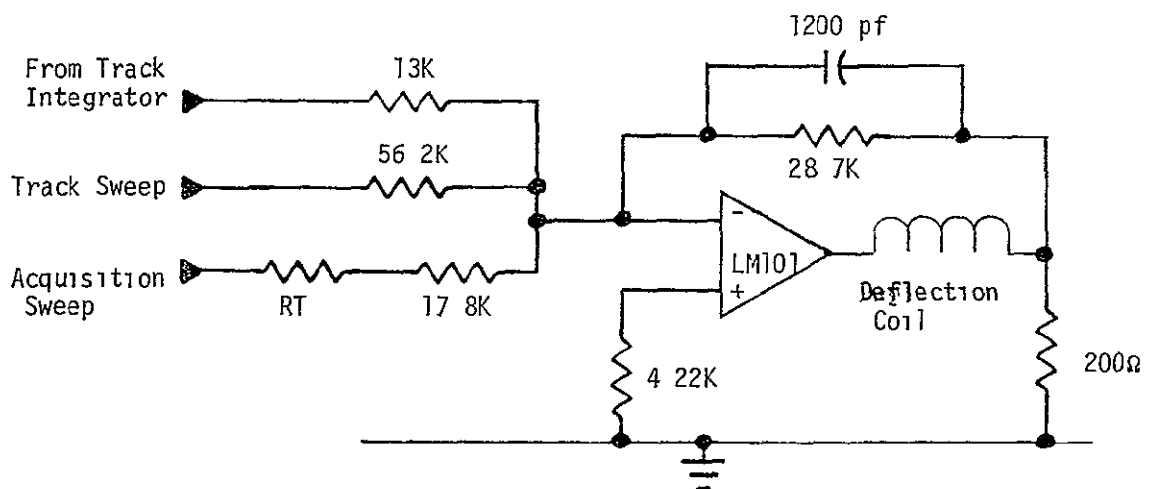


FIGURE 2-24 Coil Drive Amplifier

Coil Drive Amplifier

The phototube deflection coil is driven from a multi-input operational amplifier stage which is connected as a current driver providing a constant current drive for a given input voltage (i.e., scale factor is ma/volt)

The amplifier operates in the inverting mode and sums the following inputs

- a) Track scan waveform
- b) Track integrator dc level
- c) Acquisition scan waveform

A precision 200 ohm current sensing resistor in series with the deflection coil provides the amplifier feedback voltage

This resistor also provides a pickoff point for the output error voltage to the error amplifier and filter

Error Amplifier

The dc voltages developed across 200 ohm resistors in series with the phototube deflection coils represents the X and Y output error voltages

The two error amplifiers provide filtering to remove the track scan modulation and gain to establish the unit output scale factor of 20 millivolts per arc second

The error amplifiers consist of LM101 integrated circuit operational amplifiers connected as active filters providing a dc gain of 3.7 with a single order break at 25 Hz and a slightly underdamped second order break at 87.4 Hz

During the acquisition mode, FET switches are used to short the op-amp amplifier feedback resistor to hold the outputs at zero volts until switch over to the track mode

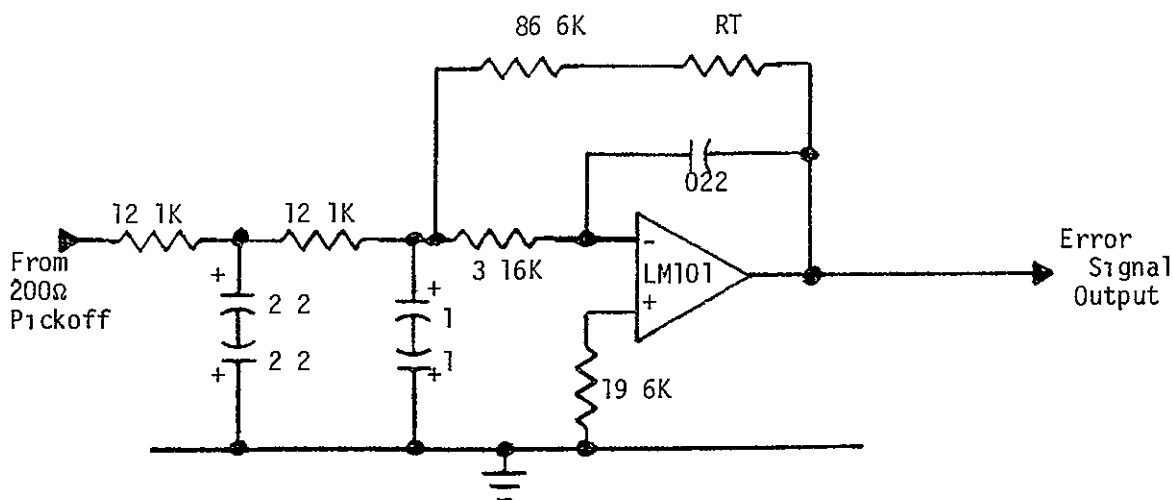


FIGURE 2-25 Error Amplifier

Mode Control Logic

The mode logic provides control of the sensor operational mode, track or search

The basic input which causes switch over to the track mode is the output of the video processor acquisition threshold detector. Video signals which exceed the acquisition threshold are stretched to a 15 millisecond width by a MSMV (Figure 2-26) and are used to set an acquisition enable flip-flop

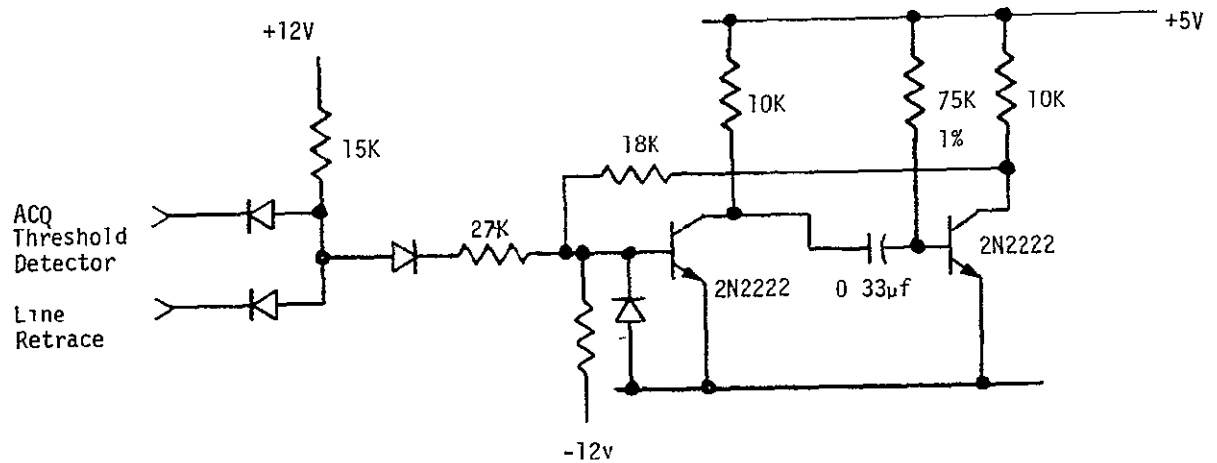


FIGURE 2-26 Video Monostable Multivibrator

This video is also sent to a video selection NAND gate which is enabled during the acquisition scan frame following the frame in which the enable flip-flop was set

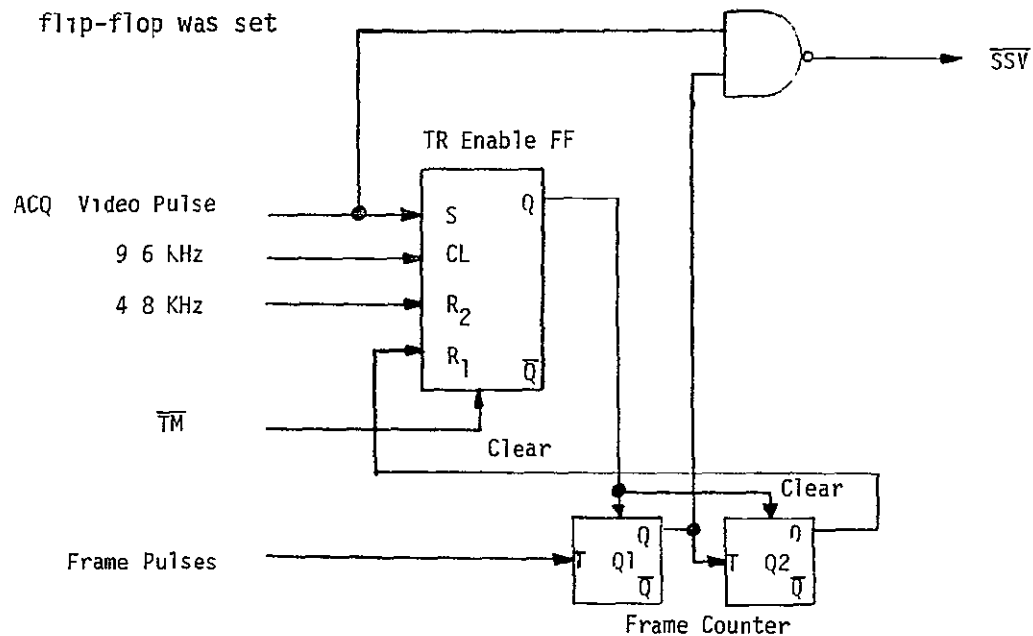


FIGURE 2-27 Acquisition Video Delay

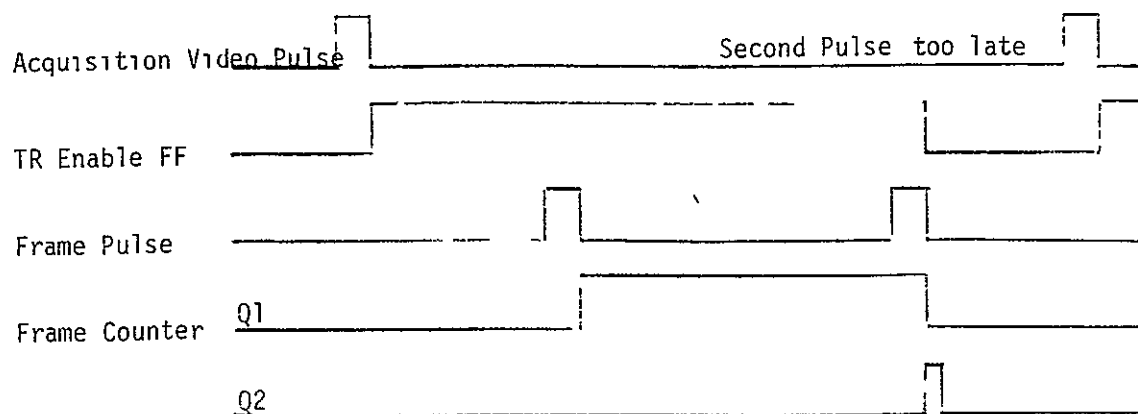


FIGURE 2-28A Timing for No Acquisition

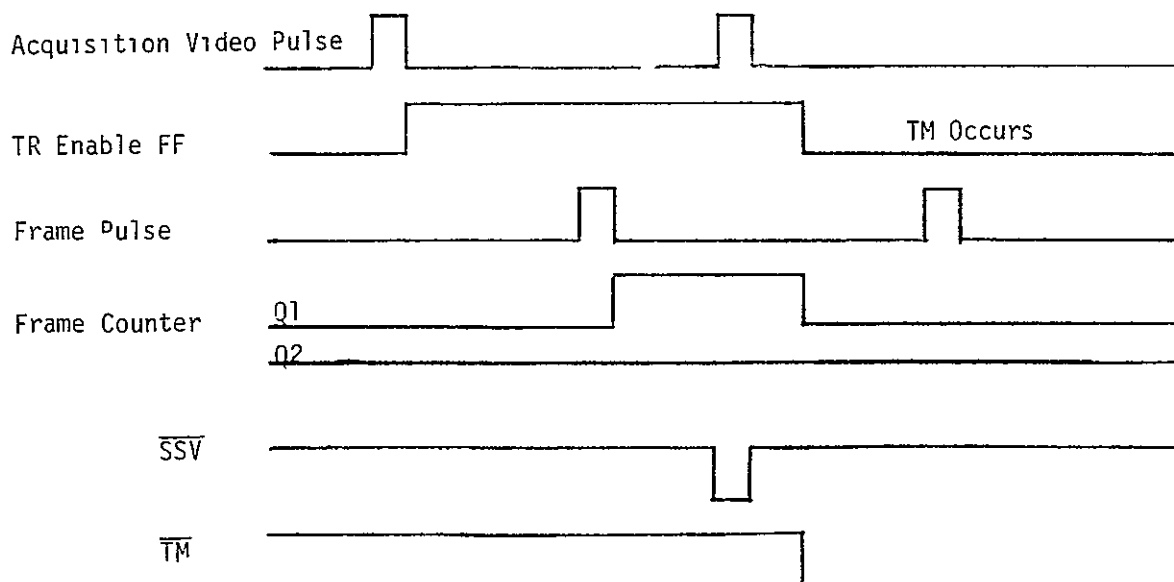


FIGURE 2-28B Timing for Acquisition

A scan frame counter Figure 2-25, provides the timing of video selection gate turn on. A complete timing diagram of operation is shown in Figure 2-26. Basically the function provided is that operation will not switch from the search mode to the track mode until a video signal exceeding the threshold has occurred on two successive frame scans.

When a video signal occurs during the proper scan interval, it is gated to the mode flip-flop to cause a switchover to the tracking mode.

For operation to remain in track, a star presence logic signal must be generated before the end of the 15 millisecond pulse interval. The input logic equations for the mode flip-flop are

$$\text{Switch to Track} = \overline{\text{CS}} [\text{SSV} + (\text{SP} \cdot \text{TM})]$$

$$\text{Switch to Acquisition} = \text{CS} + [\overline{\text{SSV}} \cdot \overline{\text{SP}}]$$

where

CS = Externally provided logic command which can force operation into the search mode when in the logic "1" state

SP = Star Presence when in a logic "1" state

TM = State of Mode flip-flop indicating operation is in the track mode

SSV = Selected Star Video. This is a logic signal which is the stretched acquisition video signal output of the video selection gate.

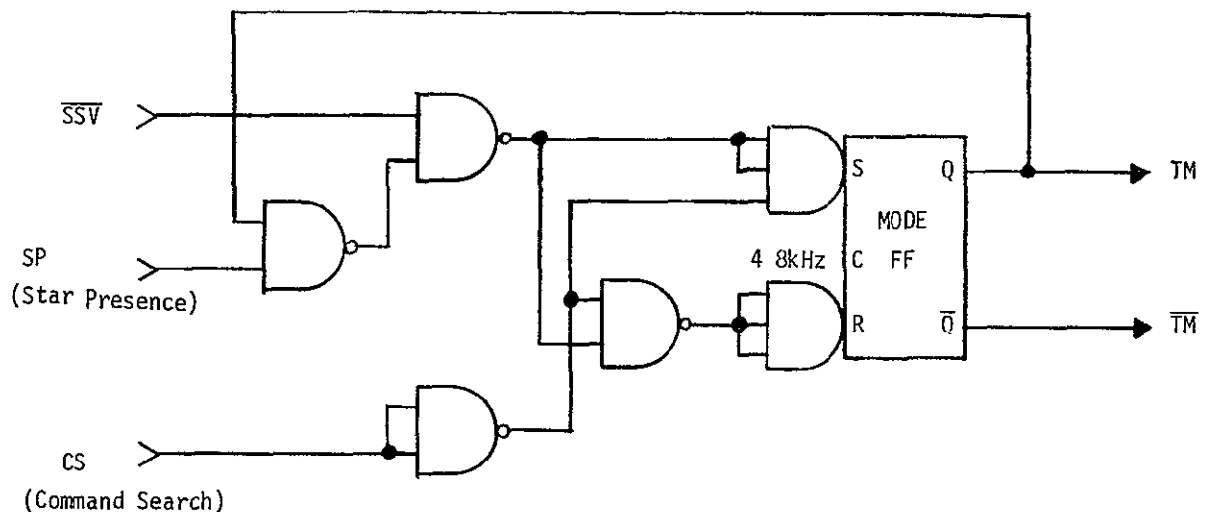


FIGURE 2-29 Mode Flip-Flop Gating Logic

12 Volt Regulators

The incoming ± 15 volt lines are regulated to ± 12.0 volts by conventional series pass regulator circuits

The regulator circuit consists of an operational amplifier, a voltage level shift zener diode and an output emitter follower

The regulated output is fed thru a resistive divider to the operational amplifier input where it is compared with a reference voltage developed from a temperature compensated zener diode

The error amplifier then adjusts the output voltage accordingly

Due to the high loop gain of the LM101 very good regulation can be achieved

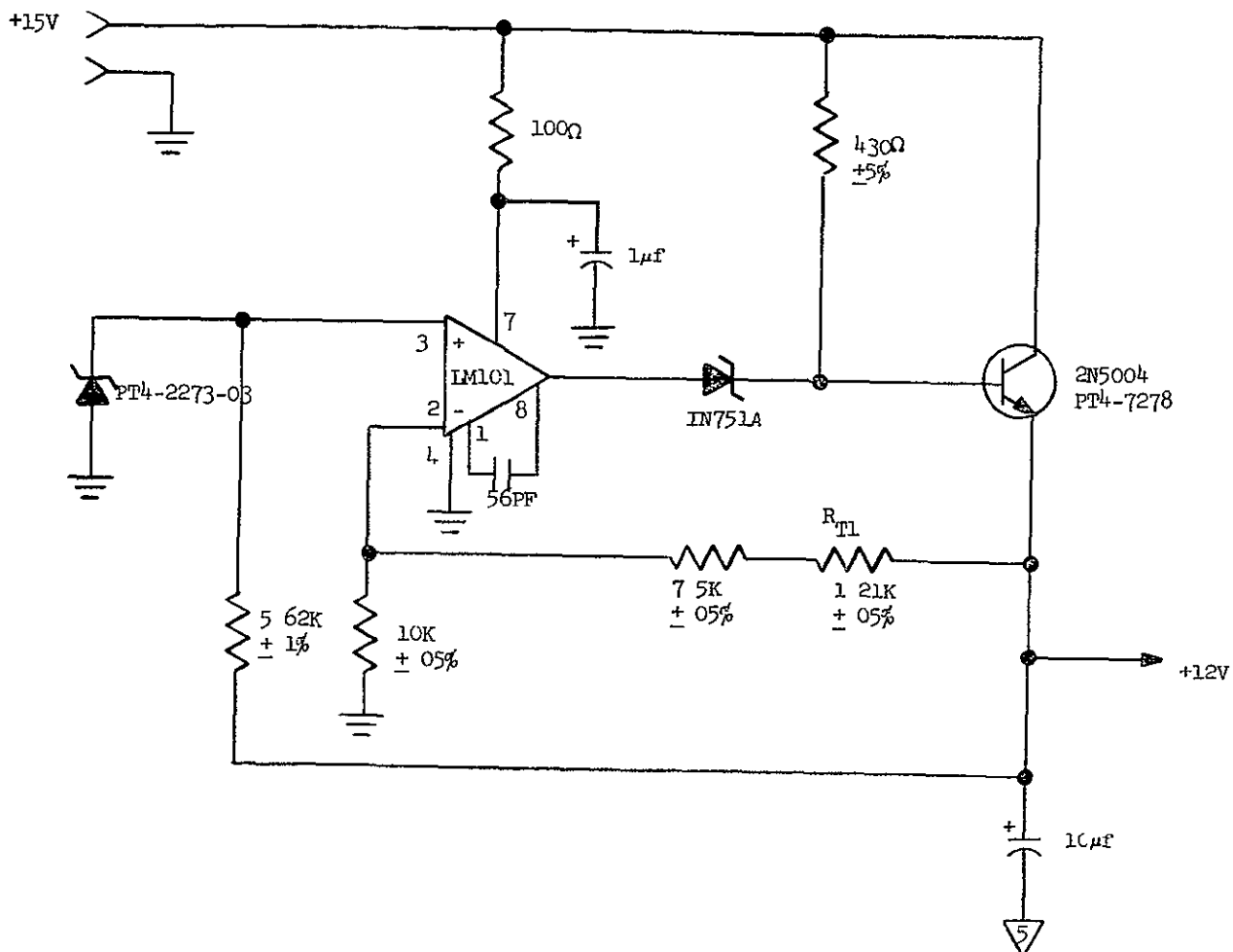


FIGURE 2-30 Plus 12V Regulator

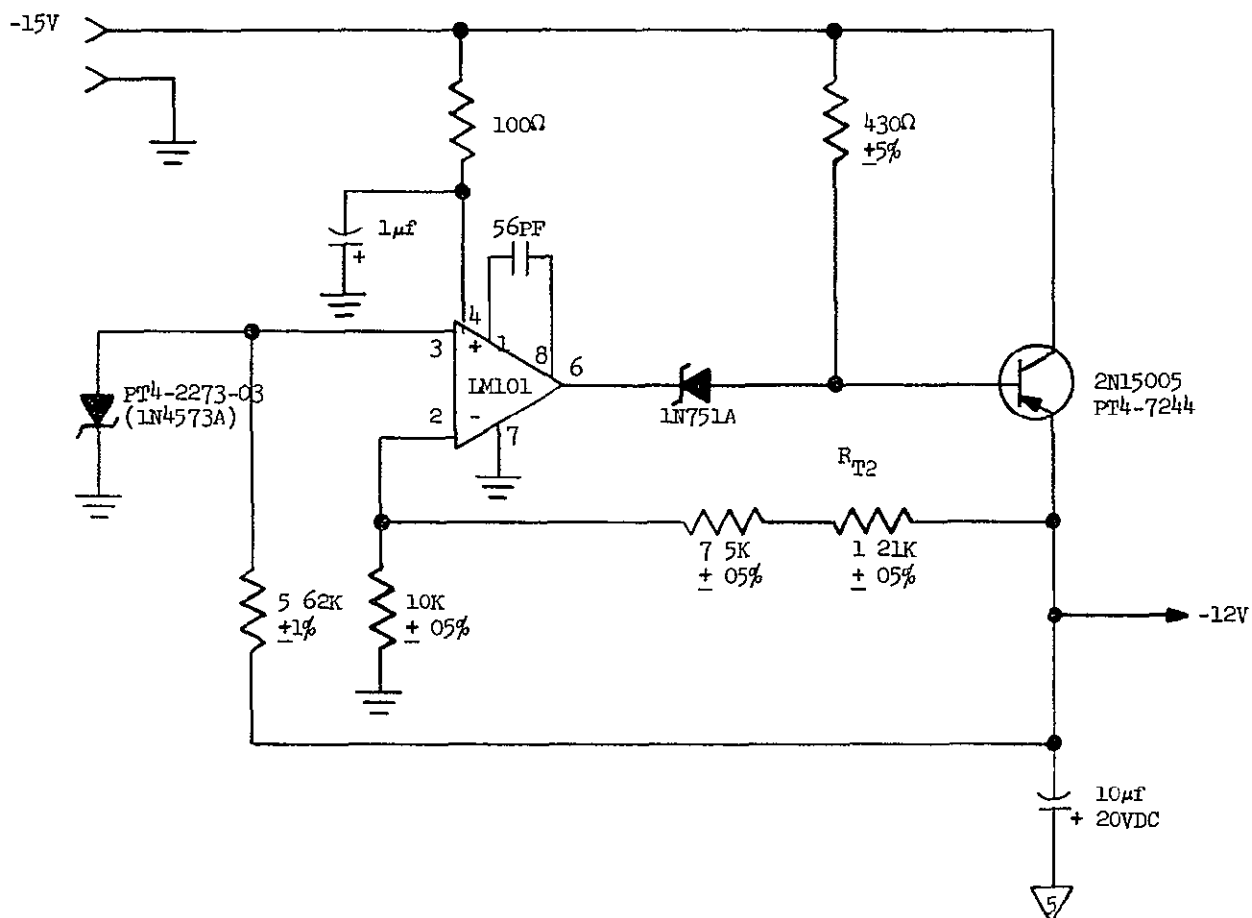


FIGURE 2-31 Minus 12V Regulator

High Voltage Power Supply and Clock Oscillator

Basic system timing is obtained from 19.2 kHz relaxation oscillator circuit which is part of the high voltage power supply.

The 19.2 kHz clock is generated by using an I C operational amplifier connected as an RC astable multivibrator. The op-amp is followed by a 2N2222 drive stage which establishes the 0 to 5 volt logic level.

The high voltage is developed in the secondary circuit of a transformer whose primary is driven at a 9.6 kHz rate by two 2N3501 transistors. The transistor base drivers are obtained from opposite sides of an I C flip-flop which is toggled by the 19.2 kHz clock.

The transformer secondary voltage is nominally 500 volts peak to peak. This voltage is quadrupled in a standard Cockroff-Walton voltage multiplier to -2000 volts unloaded.

The secondary high voltage is actually regulated to -1800 volts as is described below.

The actual load current through the phototube dynode resistors is sensed by a comparison operational amplifier stage which compares the sensed voltage with a zener voltage. The difference voltage at the operational amplifier output then drives a series pass transistor which controls the voltage applied to the primary of the high voltage switching transformer.

Bright Object Sensor Circuit

The bright object sensor consists of a Cadmium Sulfide photoconductive cell as the detector, a LM101 operational amplifier as a bridge circuit unbalance detector, a coil drive transistor, and a rotary solenoid shutter mechanism which blocks light entry to the SSU photomultiplier when activated.

The Cadmium Sulfide photoconductive cell is biased from the +12 volt supply through a series resistor with the common point of the voltage divider connected to the inverting input of an operational amplifier. The non-inverting input of the amplifier is biased to a fixed positive voltage by a resistive divider network. Then when the photocell resistance is reduced by illumination, the operational amplifier will switch to positive saturation, biasing the output transistor on, closing the rotary solenoid shutter.

Resistor values are selected such that switching occurs when the cell resistance is approximately 7K ohms (@ an illumination of 2 foot candles).

Three percent switching hysteresis is provided by positive feedback from the op-amp output.

A logic level output is also provided which switches the SSU photomultiplier high voltage off when the shutter solenoid is activated.

31,32 Missing

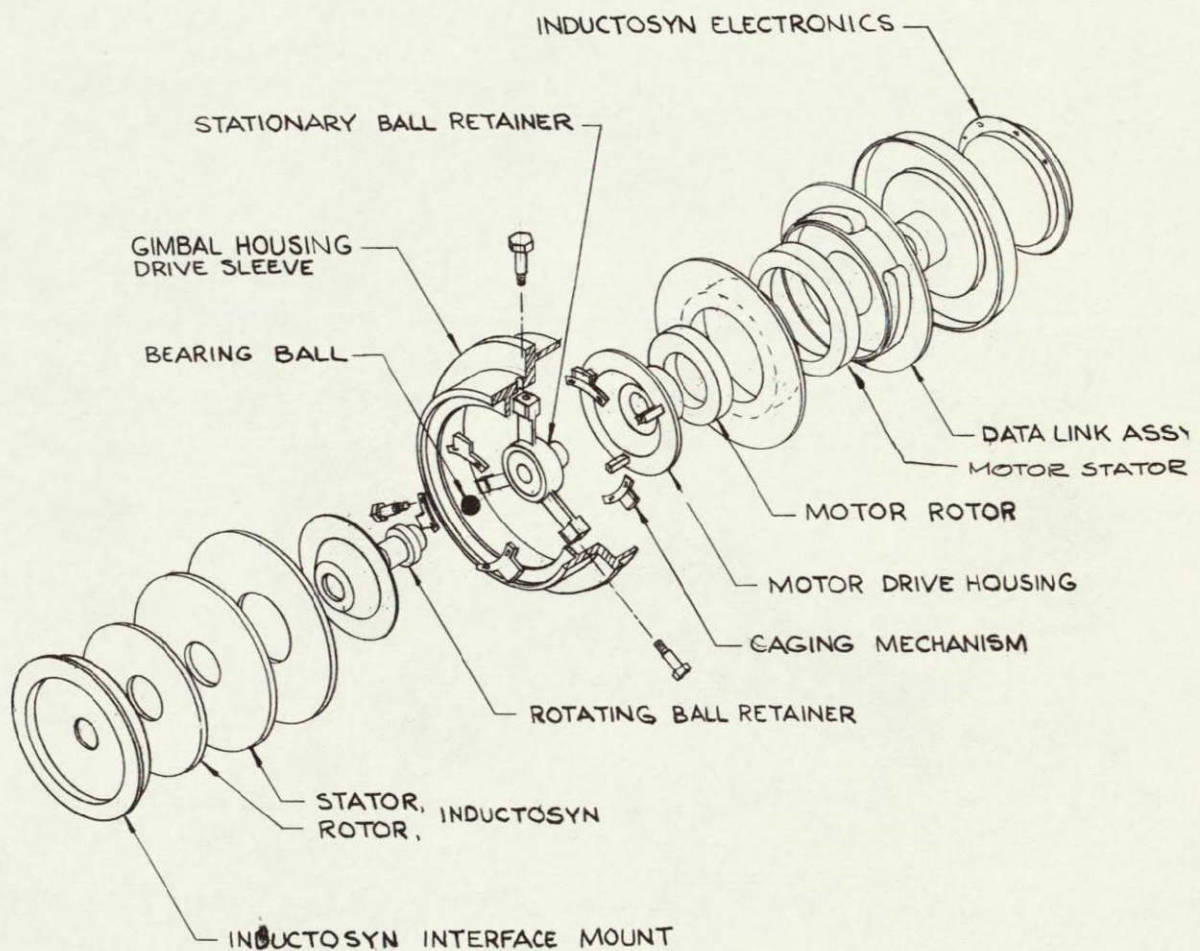


FIGURE 2-34. Star Tracker Gimbal Drive

Bearings

The bearings (Figure 2-35) consist of Stellite 6B retainers and tungsten carbide balls. Carbide was chosen for its hardness, known dimensional stability and relatively good porosity. Stellite 6 B was selected mainly to obtain reasonable hardness and the magnetic properties desired. The Stellite alloy limits the magnitude of loading by virtue of its lower compressive strength when compared to the ball material. Some of the salient characteristics of both materials are listed.

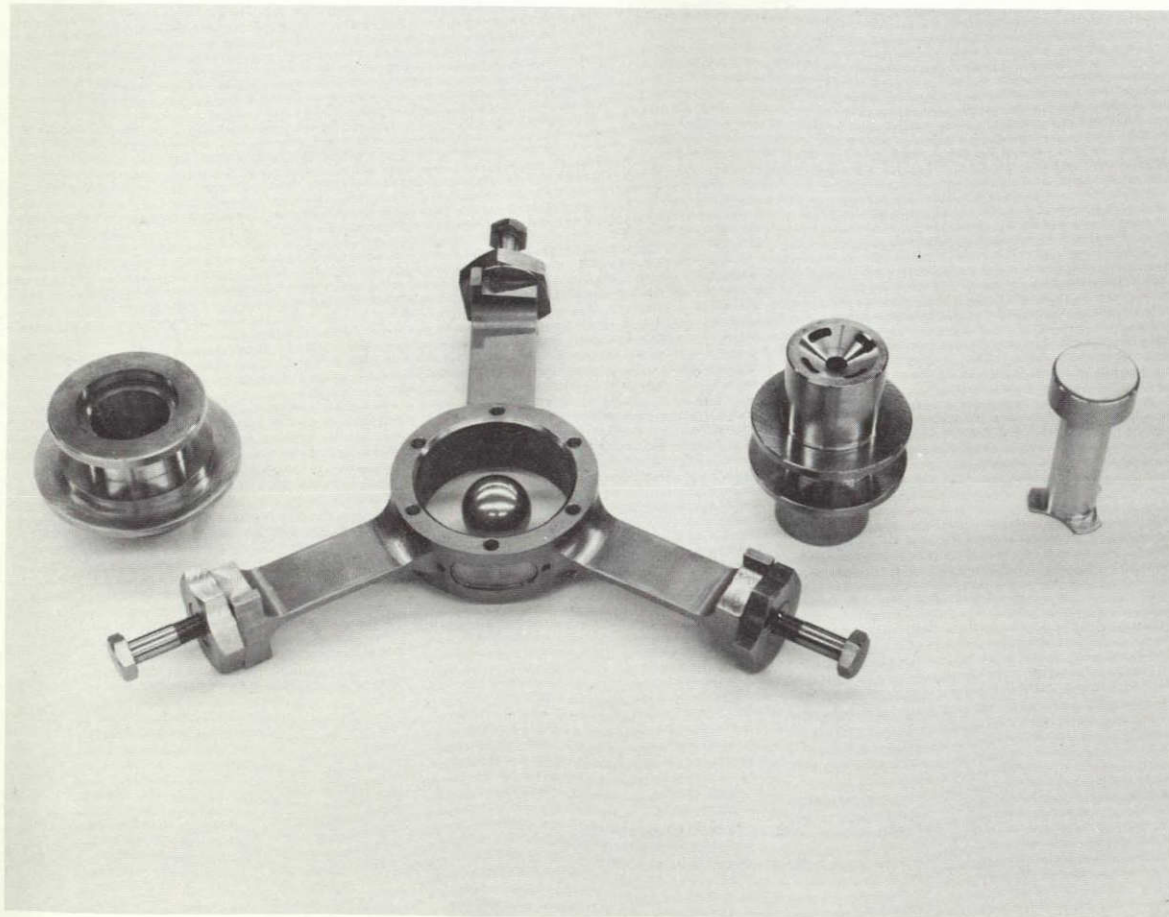


FIGURE 2-35. STA Bearings and Flexure Support

o Stellite Alloy No. 6B (Haynes)

| | |
|------------------------------|---|
| Density | 0.303 lb/in ³ |
| Specific heat | 0.101 BTU/lb/°F |
| Thermal coef. expansion | 7.7 in/in/°F x 10 ⁻⁶ |
| Modulus of elasticity | 30.4 x 10 ⁶ lb/in ² |
| Rupture | 388 x 10 ³ lb/in ² |
| Tensile strength | 165 x 10 ³ lb/in ² |
| Compressive strength | 347 x 10 ³ lb/in ² |
| Permanability @ 2000 ersteds | < 1.2 |

o Bearing Balls

| | |
|---------------------------------------|--|
| Compressive strength | 700 x 10 ³ lb/in ² |
| Modulus | 30 x 10 ⁶ lb/in ² |
| Ball size (as certified): diameter | 0.750000 in |
| Deviation in roundness | 0.000002 in |
| Finish | 0.000001 in |

Maximum bearing loads during launch vibration are 250×10^3 psi and occur on a region of the ball and retainer not used during normal operation, due to the nutating line of contact.

Lubrication

A liquid lubrication system using Krytox 143AC oil is used. The lubricant is provided to the bearing balls and the rotating retainer by a Nylasint reservoir located inside a shaft comprising a portion of the retainer element. The volume of the reservoir is 16.3 cm³ and is sufficient for a 250 year-life when initially saturated with oil. Physically, the reservoir is held against the wall surface opposite to the surface containing the line of contact that the bearing makes with its mating retainer. The molecules of lubricant are supplied to the space surrounding the ball and the retainer through holes in the retainer. There are four elongated holes surrounding the ball surfaces below the line of contact. The first set of holes represents an area of 0.48 cm² and the inner hole has 0.22 cm² cross section. The holes are filled with matching shapes of Nylasint material. This configuration affords flow of lubricant directly into the bearing chamber by wicking action, thus eliminating the molecular flow lubricating process.

The ball retainer has an included cone angle of 120° arc. This cone is inclined with respect to the center of rotation by an angle of 40' of arc. The purposeful inclination of the retainer cones provides the facility of lubrication of all the sliding surfaces by virtue of continually changing (nutating) the circle of contact. Because the line of contact nutates for the caged condition (which requires excursions greater than the operational angular displacements), Brinelling (should it take place) occurs in contact regions which are never operationally used.

Krytox 143 AC is a product of E. I. DuPont De Nemours and Company. Krytox is the designation for a family of several proprietary lubricants with different molecular weights. Krytox 143 AC fluid is a perfluoro-alkylpolyether. The oil is a colorless, odorless, completely fluorinated organic polymer. It is resistant to heat, decomposing slowly above 750°F entirely to gaseous products without appreciably altering the characteristics of the remaining fluid. The physical properties are tabulated below:

Typical Properties of Krytox^R 143 Fluorinated Oils*

| <u>Property</u> | <u>Krytox 143 AC</u> |
|---|--------------------------|
| Viscosity, centistokes | |
| @ -40°F | -- |
| @ -25°F | -- |
| @ 0°F | 33,000 |
| @ 100°F | 270 |
| @ 210°F | 26 |
| @ 400°F | 3.9 |
| @ 500°F | 2.1 |
| Viscosity Index, ASTM D2270 | 134 |
| ASTM Slope | 0.589 |
| Pour Point, ASTM D92 | -30°F |
| Density, lbs/gal @ 75°F | 15.9 |
| Density, grams/ml @ 75°F | 1.90 |
| grams/ml @ 210°F | 1.77 |
| grams/ml @ 400°F | 1.59 |
| Thermal coefficient of expansion. | |
| vol/vol/°F, Average for 77 - 210°F ($\times 10^{-4}$) | 5.7 |
| Specific Heat, Btu/lb/°F | |
| @ 100°F | 0.226 |
| @ 210°F | 0.252 |
| Thermal Conductivity, Btu/hr(ft) ² (°F/ft) | |
| @ 100°F | 0.054 |
| @ 300°F | 0.051 |
| @ 500°F | 0.051 |

| | |
|--|---------------|
| Approximate Boiling Range, °F @ 0.8 mm Hg. | ** |
| Volatility, D972 MOD.; wt % loss; 6 1/2 hrs | |
| @ 300°F | -- |
| @ 400°F | 1 |
| @ 500°F | 4 |
| Flammability | Does not Burn |
| Isothermal Secant Bulk Modulus, psi | |
| @ 100°F, 5,000 psig | 155,000 |
| Surface Tension, dynes/cm @ 78.8°F | 19.6 |
| Thermal Decomposition Point, °F | |
| Differential Thermal Analysis | 880 |
| Isoteniscope | 670 |
| Refractive Index, n_D^{25} | 1,301 |
| Electrical properties at room temperature | |
| Dielectric Strength, KV/0.1" ASTM D877-49 | 41.1 |
| Specific Resistivity, | |
| Ohm-cm x 10^{-14} , ASTM D257-61 | 4.1 |
| Dielectric Constant, ASTM D150-59T @ 100 kHz | 2.15 |
| Dissipation Factor, %, ASTM D150-59T @ 100 kHz | 0.007 |
| Vapor Pressure, mm of Hg | |
| @ 300°F | -- |
| (Isoteniscope method used | |
| on degassed samples) | |
| @ 400°F | 0.3 |
| @ 500°F | 2.9 |
| @ 600°F | 19.3 |
| @ 700°F | 165.0 |

* Technical Bulletin, DuPont, No. L5.

** Incipient decomposition begins before distillation is complete.

Flexure

The flexure (Figure 2-35) provides a bearing suspension which minimizes bearing preload changes due to temperature variation and provides a mechanism for caging and vibration snubbing. The flexure consists of a hub with a bore which accepts the stationary bearing retainer. The hub is supported by three flexure elements located 120 degrees apart. Each element has a cross section of 0.1 x 0.75 inches and is made of titanium. The outboard end of the flexure has a solid section of which two sides are flat and the sides perpendicular to the axis of rotation are tapered. These tapers match stops mounted on the rotating shaft when the gimbal is rotated to its maximum angle, thus providing axial caging. A clearance of 0.002 inch is maintained. Radial stops are provided by the inner surface of this outboard end of the flexure.

The solid section of the flexure terminates with a double threaded boss. The internal thread is used to provide radial tension to the flexure by preloading against the drive assembly housing. The outer thread is used to lock the preload bolt to the housing and to preload the bolt. A summary of flexure characteristics is listed below:

Preload Flexure

| | |
|--------------------------|--|
| o Material | Titanium |
| o Stiffness | |
| Axial (K_y) | $10^4 \frac{\text{lb}}{\text{in}}$ |
| Lateral (K_x) | $0.375 \times 10^6 \frac{\text{lb}}{\text{in}}$ |
| Lateral (K_z) | $10^6 \frac{\text{lb}}{\text{in}}$ |
| Radial @ 120 deg | $0.250 \times 10^6 \frac{\text{lb}}{\text{in}}$ |
| Radial (Preloaded) | $5.3 \times 10^6 \frac{\text{lb}}{\text{in}}$ |
| Torsional (K_θ) | $26 \times 10^3 \frac{\text{in-lb}}{\text{rad}}$ |
| o Stresses (Max) | |
| Axial (bending) | $9,400 \text{ lb/in}^2$ |
| Radial preload | $8,000 \text{ lb/in}^2$ |
| Lateral (x) | $9,500 \text{ lb/in}^2$ |
| Lateral (z) | $3,000 \text{ lb/in}^2$ |

Preload Flexure (cont.)

| | |
|----------------------|---|
| o Stress per arc sec | |
| Lateral (x) | 170 lb/in ² |
| Lateral (z) | 615 lb/in ² |
| Torsional (θ) | 141 lb/in ² |
| o Forces per arc sec | |
| x Direction | 5.7 lbs |
| z Direction | 57.0 lbs |
| o Caging | |
| o Stiffness | |
| Radial | $5 \times 10^6 \frac{\text{lb}}{\text{in}}$ |
| Axial | $0.4 \times 10^6 \frac{\text{lb}}{\text{in}}$ |
| Max. Stress (bolt) | 41,000 lb/in ² |

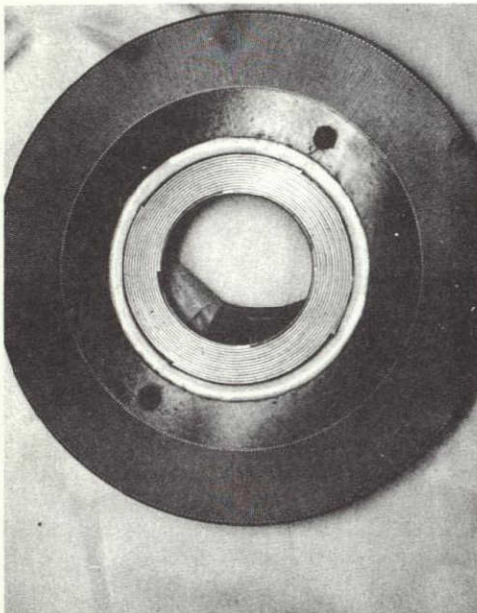
Motor

The gimbal drive motor is a permanent magnet dc machine. It has two-phase windings with a common return and has linear dc torque-speed characteristics when commutated as a 12 speed device. The motor has 24 poles, 2 slots per pole, its ID is 2.758 inches and its OD is 4.6594 inch. A summary of characteristics is listed below:

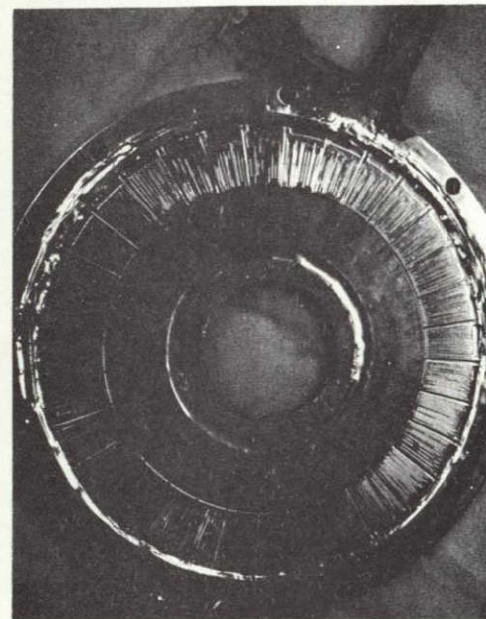
| | |
|-----------------------|------------------------|
| Manufacturer | Schaeffer Magnetics |
| Torque Constant | 180 in-oz/amp |
| Speed Constant | 0.7 volt/rad/sec |
| Cont. Torque | 60 oz-in |
| Max. Torque (Stall) | 1.2 ft-lb |
| Torque Ripple | < 3 in-oz |
| Air Gap (min) | 0.006 in |
| Weight | 2003 |
| Insulation Resistance | 100×10^6 ohms |
| Dielectric Strength | 500 v. RMS @ 60 Hz |
| Resistance | 54.5 ohms |
| Power @ 60 oz-in | 6 watts |
| Nominal Power | 1.5 watts |
| Residual Torque | 2 oz-in |
| Magnetic Leakage | 3 gauss @ 1 in |

Inductosyn

The gimbal angle encoder used is an Inductosyn^R, manufactured by Farrand. The Inductosyn^R is a pair of discs mounted to rotate coaxially with facing surfaces in close proximity. The facing surfaces have printed conductors arranged to form winding circuits which are linked, disc-to-disc. A single winding is formed on the rotor. The stator has a sine and cosine winding of 720 poles and another set of 2 poles. The resulting device is similar to multispeed synchro resolver with low coupling.



R O T O R



S T A T O R

FIGURE 2-36. STA Inductosyn Plates

Figure 2-36 shows the Inductosyn. The windings are printed on an aluminum plate and covered with a shield, as shown. Typical characteristics are listed below:

| | <u>360 Speed</u> | <u>Single Speed</u> |
|--|-------------------|---------------------|
| Accuracy | ± 1.6 arc sec | ± 18 arc min |
| Phase Shift @ 10 KHz | 890 | 750 |
| Rotor Impedance | $15.5 + j 2.6$ | 1.313 |
| Stator Impedance | $5.5 + j 1.2$ | 0.5 |
| Nominal Gap | .007 inch | 0.007 inch |
| Transformation Ratio (@ 0.01 in. gap) | 2000/1 | 1050/1 |
| Power (Excitation) | 2 watts | 2 watts |

Data Link

The data link is shown in Figure 2-37. It consists of a larger diameter stationary member attached to the gimbal drive sleeve and a small diameter cylindrical component, (the rotating member), attached to the motor shaft.

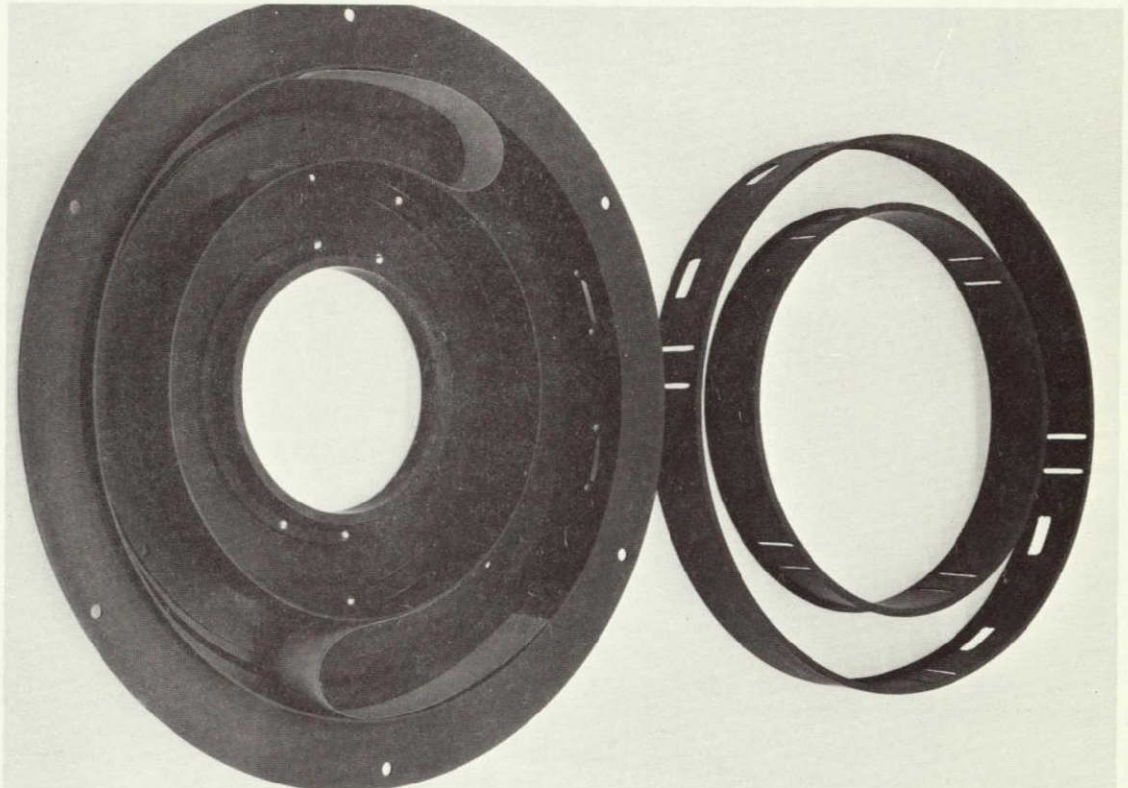


FIGURE 2-37. STA Data Link

The inner and the outer members are lined with nylon rings to provide electrical insulation and mechanical guide for the rollamatic action of a 11 conductor strip. There are 4 such strips providing the capability of $\pm 60^\circ$ motion with restraint torque not exceeding 1/2 in-oz. Both the stationary and the rotating members of this assembly are made from aluminum alloy. Miniature electrical connectors are attached to the peripheries of the rotating and stationary component. The assembly itself is so designed that it can be removed from the system without disturbing the various electrical interconnections.

Manufacturer

Hughes (PN 4000855)

Physical Characteristics

| | |
|------------------------------|--------------------|
| o No. of conductors | 11 |
| o Type of conductor (cu) | 0.003 x 0.025 inch |
| o Spacing between conductors | 0.050 inch |

- o Insulation:
 - 1 layer FEP adhesive (thickness) 0.002 inch
 - 2 layer of Kapton shield (thickness) 0.002 inch ea.
 - Spray coated silver Epoxy (DuPont A5504) 0.001 inch
- o Grounding
 - Shield is grounded to one of the conductors at intervals of 2.0 inch
- o Temperature 200°C to -50°C

Electrical Characteristics

- o Current Capacity 2 amps per conductor
- o Insulation resistance 75 volts/mil

Crosscoupling noise:

(The following are experimental comparison data for a 26 inch long strip and a 0.5 v RMS input and equivalent shielded and unshielded standard electrical wires.)

| Element | CROSS COUPLING RMS VOLTS | | | Remarks |
|--|--------------------------------|--------------------------------|--------------------------------|---------------------------|
| | Frequency | | | |
| | 10KC | 100KC | 1000KC | |
| #22 Teflon insul. and shield (side by side) | $43 \times 10^{-6} \text{v}$ | $24.5 \times 10^{-6} \text{v}$ | $320 \times 10^{-6} \text{v}$ | $v_{in} = .5\text{v RMS}$ |
| #22 Teflon insulation (side by side) | $25.5 \times 10^{-5} \text{v}$ | $260 \times 10^{-6} \text{v}$ | $2100 \times 10^{-6} \text{v}$ | |
| #22 Bare copper wire 1/4 inch apart | $17.5 \times 10^{-6} \text{v}$ | $160 \times 10^{-6} \text{v}$ | $1350 \times 10^{-6} \text{v}$ | |
| Rollomatic Strip | $5.6 \times 10^{-6} \text{v}$ | $27.5 \times 10^{-6} \text{v}$ | $23.5 \times 10^{-6} \text{v}$ | |

Mechanical Characteristics

- o Stress due to bending 25000 lb/in²

3.0 Sensor Electronics Assembly

3.1 Function

The Sensor Electronics Assembly (SEA) provides the electrical interface between the Star Tracker Assembly and the Data Processing Subsystem. The SEA encodes the star tracker gimbal angles (from the Inductosyn signals), controls and drives the gimbal motors, and provides an A/D converter for the star sensor analog output signals.

3.2 Configuration

The Sensor Electronics Assembly is packaged according to the "slice" concept, which has been used successfully on many previous TRW programs. This approach is illustrated in Figures 3-1, 3-2, and 3-3 for a typical assembly. The electronic components are distributed on etched circuit boards, typically 5" x 7". For circuitry which is mostly composed of discrete components, a two-sided etch pattern is used. Where a high density of integrated logic circuitry is desired, multi-layer boards are used, since with merely two-sided etch, the board area required for hook-up pattern typically exceeds the area occupied by the components.

A "slice" is composed of one to three interconnected boards housed in a machined aluminum frame. Interconnections between boards within a frame are via flexprint flat cable. Thus the boards can be laid out flat for checkout, probing, and possible troubleshooting, prior to assembly into the frame. When assembled, the boards are folded and securely mounted.

Slices are assembled side-by-side to form an assembly, with end covers placed over the exposed sides of the outboard slices. Each slice carries a set of rectangular bulkhead connectors along one of its exposed faces. Interconnections between slices are made via one row of connectors, while the other row is used for the assembly interface.

The slice and board organization of the Sensor Electronics Assembly is as follows:

- Excitation and A-D
 - Excitation Board
 - A-D Converter Board
- Motor Electronics, X-axis
 - Preamp Board
 - Power Amp Board
 - Power Amp Board

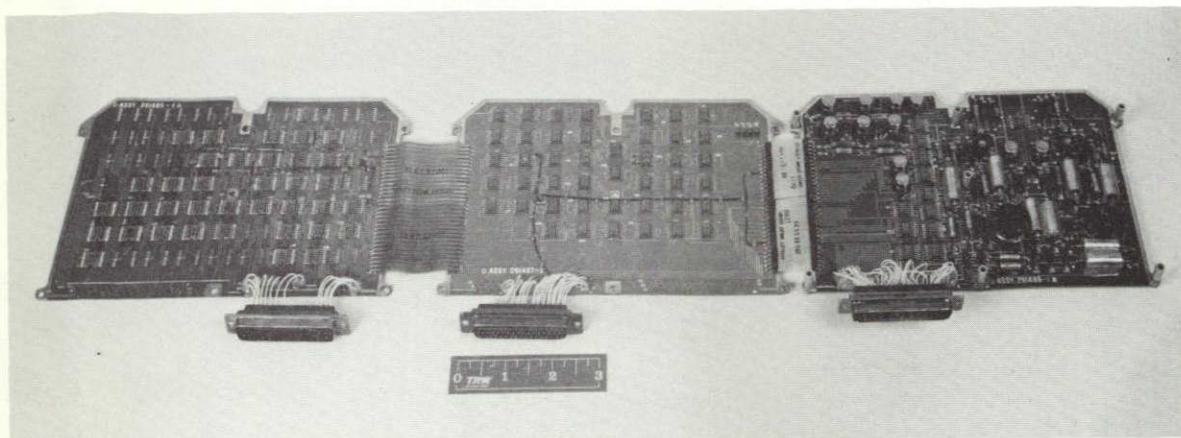


FIGURE 3-1. Circuit Boards Prior to Folding and Mounting



FIGURE 3-2. Assembled Slice

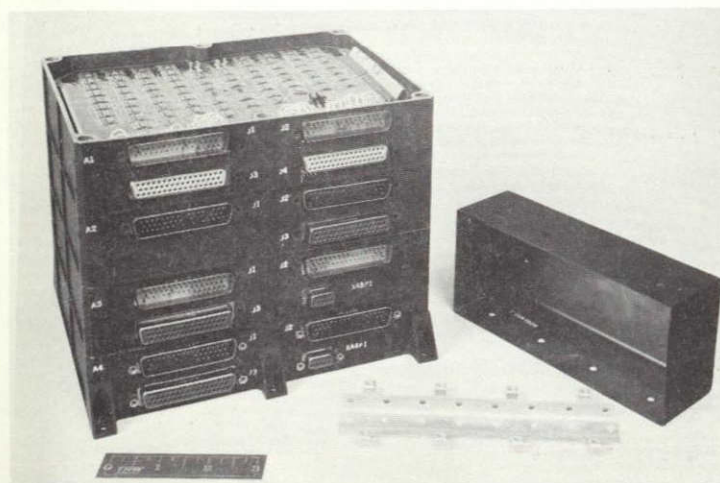


FIGURE 3-3. Slices Stacked to Form an Assembly. One Row of Connectors is for Slice-to-Slice Interconnections. Cover for this Harness is also shown.

Single-Speed Encoder, X-axis
 Analog Board
 Logic Board
 Multi-Speed Encoder, X-axis
 Analog Channel Board
 Analog Channel Board
 Logic Board
 Motor Electronics, Y-axis
 Preamp Board
 Power Amp Board
 Power Amp Board
 Single-Speed Encoder, Y-axis
 Analog Board
 Logic Board
 Multi-Speed Encoder, Y-axis
 Analog Channel Board
 Analog Channel Board
 Logic Board

The partitioning reflects a high degree of commonality. Corresponding slices for an axis are identical. In addition, the power amplifier boards of the Motor Electronics slice and the analog channel board of the Multi-Speed Encoder slice are respectively identical. Table 3-1 lists the physical characteristics for the Sensor Electronics Assembly.

TABLE 3-1 Sensor Electronics Assembly, Physical Characteristics

| | |
|---------------------|-----------------------|
| Slices | 7 |
| Boards | 18 |
| Dimensions | 8" h x 11 2" w x 6" d |
| Weight | 9.5 lbs |
| Power | 15 watts quiescent |
| Components | |
| Integrated Circuits | 322 |
| Discrete Components | 1270 |

3.3 Operational Description

Figure 3-4 is an overall block diagram of the Sensor Electronics Assembly, essentially with processing for one of the two gimbal axes shown. The major included functions are encoding of the Star Tracker gimbal angles from the Inductosyn signals, control and drive of the gimbal motors,

3-4

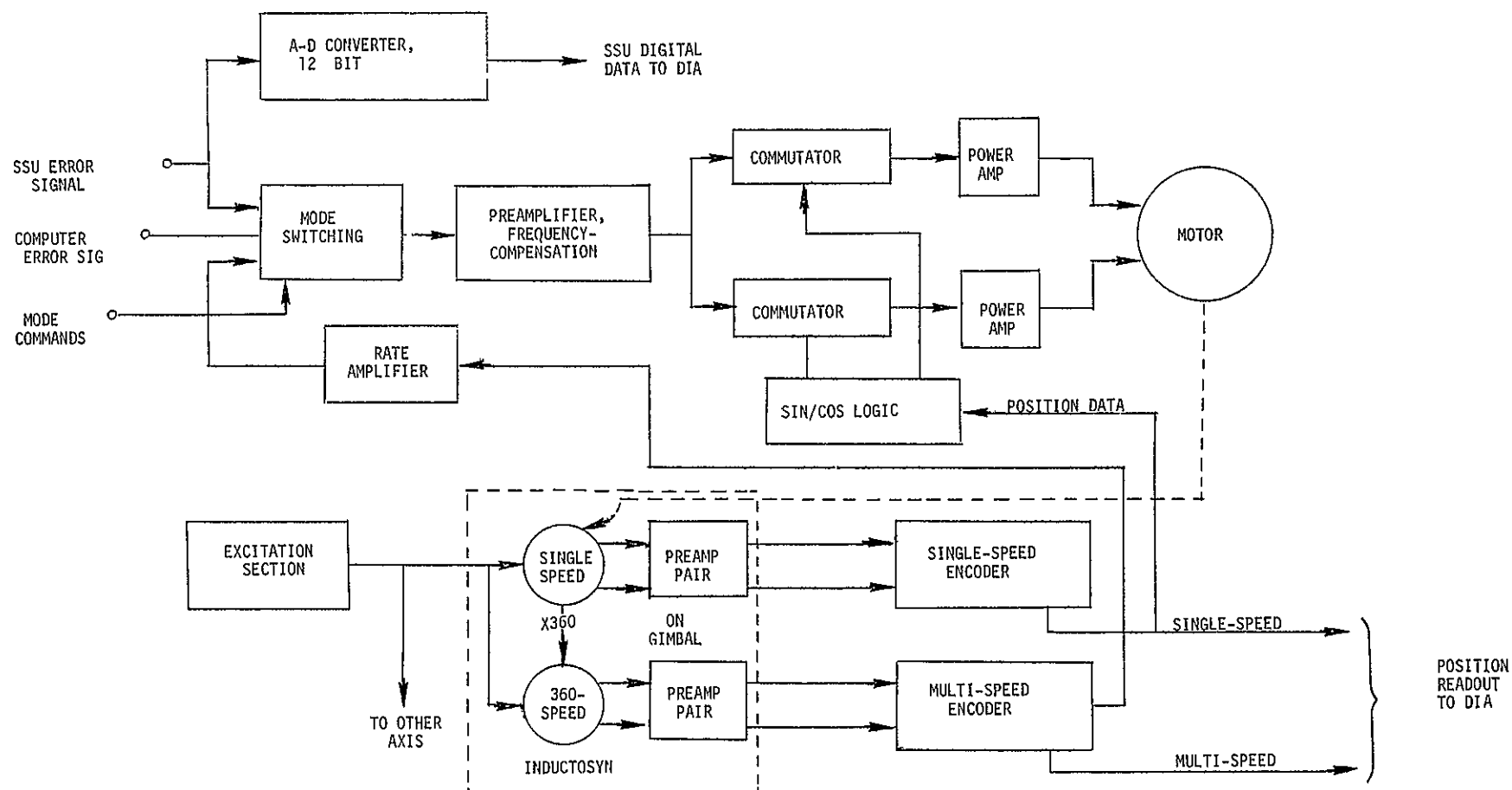


FIGURE 3-4 SEA Block Diagram

and 12 bit A-D conversion of the star sensor error signal for use by the computer

Determination of gimbal angle is accomplished by using an Inductosyn, which produces a set of signals analogous to that of a synchro resolver, but with much higher resolution. Each Inductosyn has a 360-speed section for high resolution and a single-speed section for absolute position determination unambiguously. The Inductosyn rotors are excited in parallel from the common Excitation Section by a low-distortion sinusoidal 10 kHz, which is generated as a countdown from a higher-frequency crystal controlled oscillator.

Because of their low level the Inductosyn signals are first amplified by a set of preamplifiers, located on the gimbal in the immediate vicinity of the Inductosyn. The single-speed and the multi-speed encoders convert the incoming sine-cosine amplitude data into a digital position output using a form of double-angle phase technique. Each encoder is mechanized as a pair of trigonometric phase-lock loops. An analog rate signal is also developed for local damping of the motor.

The Motor Electronics has as its function the control of the gimbal motor, including conditioning of the rate signals, frequency compensation of the motor drive function, commutation of the motor windings, and power control to the motor. There are three modes, controlled by the computer. In slew mode, the computer error signal drives the motor directly without local compensation. In acquisition mode, drive is still from the computer, but with local rate damping and the frequency-compensation (integral plus proportional) of the preamplifier added. In track mode the servo loop is closed mainly via the Star Sensor through the preamplifier, with local rate damping and with addition of the computer control signal for any bias, etc., compensation which may be necessary.

A typical sequence of operations would begin in slew, when the computer would drive the Star Tracker to the assumed angle to the desired star. During acquisition, the gimbal is driven (under computer control) in a programmed search, while the Star Sensor raster scans its deflection field, searching for the star. When the star is found, it signals the computer, and the computer switches the SEA to Track Mode. At this time the SSU error signal is used to close the gimbal servo loop tending to drive the star LOS to coincidence with the sensor's boresight. The combined gimbal angle and star sensor error is sampled by the computer. At periodic update intervals, a new star is acquired.

The motor is a 12-speed, two-phase device. To maintain torque at maximum for a given drive level, the power to the respective phases is programmed proportional to the sine and cosine of $12(\theta + 90^\circ)$, θ being the instantaneous gimbal angle. The sine/cosine logic performs the function of deriving an approximation to the sine and cosine of 12θ . As a set of digital quantities this is multiplied by the analog servo variable as it is output from the preamp. The resulting signals are power amplified and applied to the respective motor phases.

A 12-bit analog-to-digital converter is provided to encode the SSU Error Signal for use by the computer. This converter is necessary because the standard converter provided within the DIA is not of sufficient resolution and precision for this purpose. Although not indicated in Figure 3-4, a single converter services both axes on a time-shared basis. The converter is of the successive approximation type.

3.4 Performance Summary

Table 3-2 summarizes the performance characteristics for the SEA. Table 3-3 summarizes the significant error contributions for the Inductosyn processing.

TABLE 3-2 SEA Performance Summary

| | |
|---------------------------------------|---|
| <u>Inductosyn Encoding</u> | Dual speed, phaselock resolver format encoders Two axis |
| Excitation frequency (Sample rate) | 10.5 kHz |
| Phaselock loop bandwidth | 200 Hz nominal |
| Resolution | 0.23 arc sec |
| Accuracy | ± 0.6 arc sec (1σ) |
| Range | 180 degrees |
| <u>Motor Control</u> | Quadrature, 12-speed drive Electronic commutation Local rate damping and frequency compensation Two axis |
| Maximum voltage | ± 18 volts per phase |
| Delivered power | 10 watts peak per axis |

TABLE 3-2 SEA Performance Summary (Continued)

| | |
|------------------------|-------------------------------------|
| <u>A-D Converter</u> | Successive approximation, two input |
| Resolution | 1 4,096 |
| Null stability | ± 5 millivolts |
| Scale factor stability | $\pm 1\%$ |
| Range | ± 5 volts |
| Conversion Time | 50 μ sec |

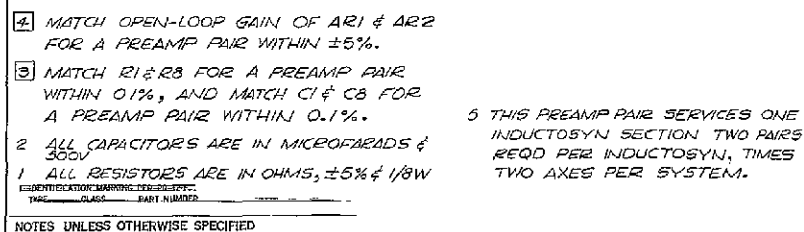
TABLE 3-3 Inductosyn Encoding Error Summary

| <u>Error Type</u> | <u>Form</u> | <u>Nature</u> | <u>Magnitude (Electrical)</u> |
|-------------------------|---|---------------|-------------------------------|
| Excitation harmonics | $\Delta\phi_e \leq \frac{\Delta V}{V}$ | Harmonic | 2×10^{-4} rad |
| Cross coupling | $\Delta\phi_c = 1/2 \frac{\Delta C}{C}$ | 2nd Harmonic | 10^{-3} rad |
| Trig gain unbalance | $\Delta\phi_g = 1/2 \frac{\Delta k}{k}$ | 2nd Harmonic | 2.5×10^{-4} rad |
| Phase detector offset | $\Delta\phi_d = \frac{\Delta V}{K_d}$ | Offset | 2×10^{-4} rad |
| Phase detector harmonic | $\Delta\phi_h \leq F_o(s)$ | 2nd Harmonic | 10^{-5} rad |
| Phase servo error | $\Delta\phi = \frac{\Delta\omega}{K_v}$ | Offset | 3×10^{-4} rad |
| TOTAL (RSS) | | | 11×10^{-4} rad |
| | | | 0.063 degree |
| | | | 3.8 arc minutes |
| 360-Speed Equivalent | | | 0.6 arc seconds |

3.5 Design3.5.1 Excitation Section

This circuit (X264480) Figure 3-5, produces a high-purity 10.5 kHz sinusoidal voltage for excitation of the star tracker gimbal Inductosyn rotors. The crystal oscillator (AR1 and associated components) operates at 1260 kHz. The oscillator output is counted down (modulo 120) to produce a special modulation function at the outputs of EQ00 Pin 12, EQ01 Pin 12, and EQ02 Pin 9. This logic function drives a 3 bit D-A converter (AR6, 7, 8) to produce a

This page intentionally left blank



| REVISIONS | | | |
|-----------|-------------|------|---------|
| LT# | DESCRIPTION | DATE | APPROVE |
| | | | |
| | | | |
| | | | |

[illegible]

FIGURE 3-6 SEA Preamplifier Pair

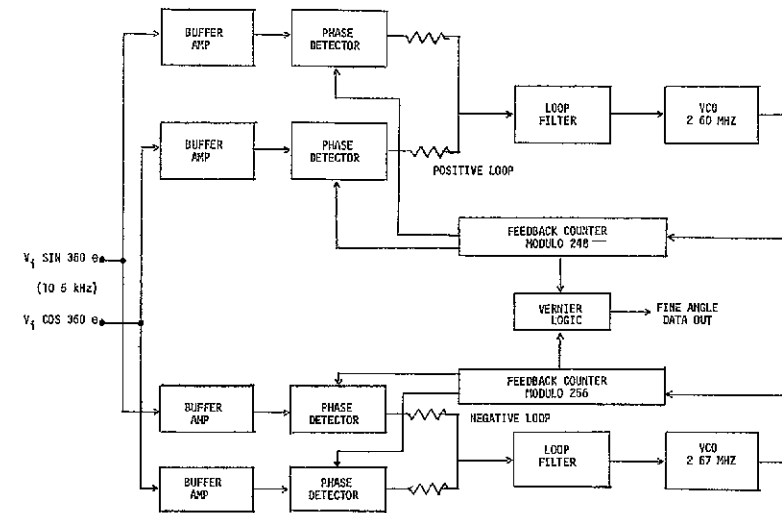


FIGURE 3-7 Multispeed Encoder

match between a sine/cosine pair at the signal frequency. Thus, the high-gain, wideband $\mu A715$ operational amplifier is again used, and the primary gain-determining components are again specified at 0.01%. The secondary gain-determining components are matched to 0.1% for a pair.

The low-frequency corner of the passband is first order, placed at approximately 100 Hz. Its purpose is to block any DC which might appear in the preamp output due to preamp offset voltage. While the phase-locked loop is not sensitive to input DC, its presence at this point would be inconvenient in that its magnitude could be of the same order as the working signal. The high-frequency corner is second-order, with nominally critical damping, placed at approximately 100 kHz, a decade above the signal frequency. Its placement is a compromise between a desire to limit possible noise frequencies outside the signal band and a desire to minimize the effect of capacitance value drifts on 10.5 kHz gain. Again, the power voltage isolation (e.g., R4, C4, C8, R6, C7, C10) is very conservative to prevent possible cross-talk via the power lines from sine to cosine and from loop to loop.

Note that the combination R95, C70 forms a first-order lag at 200 Hz to the input control signal. The circuit is designed to oscillate at approximately 2.6 MHz. The zero-input frequency is trimmed to 2.60 MHz and 2.67 MHz, positive and negative loops respectively, by selection of R98 and R108. R95 is chosen so as to give the device a gain of approximately 1.25% frequency variation per volt at the output of AR8.

The VCO output drives the synchronous feedback counter. The design of both counters is identical except for the position of the jumper wire at the input of MC07/, MC57/ (the "slash", "/", is used herein to designate the logical complement of a binary variable, i.e. the "bar"). For the positive counter, the jumper makes a modulo 31 of the MC03 through MC07 stages. For the negative counter, the corresponding stages, MC53 through MC57 form a modulo 32. For both, the last 3 stages form a modulo 8.

The last two stages, e.g., MC00, MC01 are a modulo 4 Gray code sequence, i.e., the sequence desired to drive the respective sine and cosine sections of the phase detector.

Because the phase-feedback action of the phaselock loop is such that the output of the feedback counter must match the loop's input frequency cycle-for-cycle, then the VCO frequency must be precisely M times the input frequency, where M is the feedback counter modulus. Since the two counters differ by 31/32 in their frequency division factors, then the VCO's must differ by precisely this ratio. Thus, they will have some relative precession which recurs 8 times per counter revolution. MQ20 and MQ21 form a sequencer which detects when the two VCO's are exactly in phase in the one precession cycle per major revolution when readout is desired. At this instant the signal MK20 causes the contents of both counters to be read into the double buffer register MR20 through MR27.

The combined contents of these two registers contains both coarse and fine data. Coarse data appears directly in MR20 through MR27, except that the Gray code format of the two most-significant bits is converted to binary via the gating structure culminating in MD20 and MD21. Fine data appears implicitly as the difference between the contents of MR22 - MR27 and MR52 - MR57. This differencing is performed via a parallel subtractor, culminating in MD22 through MD27.

3.5.4 The Single-Speed Encoder

The single-speed encoder, drawing X264479, Figure 3-9, is a somewhat simplified version of the multi-speed. In most cases, the simplifications are possible because this section does not require the same order of accuracy

This page intentionally left blank

Each of these signals is amplified using a DC coupled, class AB power amplifier, similar to the one used in the excitation section, and the results are applied to the respective motor phases

3 5 6 Analog-to-Digital Converter

Because the standard A-D converter within the Digital Interface Unit does not have sufficient resolution to encode the Star Sensor X and Y axis signals, it is necessary to provide a special converter for this purpose. The sensor signal is scaled at 20 mv per arc second. The A-D converter is scaled at 12 bits over a range of ± 5 volts, or 2.5 millivolts per quanta. The resolution is then 1/8 arc second, and the linear conversion range is ± 250 arc seconds. In this application where operation is with respect to null, the converter is required to have good null accuracy but the scaling accuracy is not of great importance.

The converter schematic appears as drawing X264481, Figure 3-11. It is a successive approximation converter, using a D-A conversion system by Analog Devices, Inc.

The buffer amplifiers receive the respective X and Y axis sensor signals. The buffer gain is unity. The signals are received and buffered in two-wire differential form to remove the effects of any possible common-mode ground potential difference between the Star Sensor and the SEA. The buffered signals are passed to the motor electronics for use in controlling the gimbal servos, as well as used internally for conversion.

The converter proper is time-shared between the two axes. Control commands (DK60 and DK61) are received from the DIA to initiate conversion and to specify which axis is to be converted. The axis to be converted is switched into the converter by the DG144 solid-state analog switch.

The μ DAC550 modules are D-A current switches. Each module has 4 bits. The current contribution of each bit to the #8 pin output of each module with a LOW digital input for that bit is binary scaled by the associated resistor (10K, 20K, etc.) within the thin-film resistor module (C-4153). The most-significant module connects its current directly to the summing node of the comparator, the LM111 (National Semiconductor). The output currents of the two lesser-significant modules are attenuated respectively by 1/16 and 1/256 by a current dividing network within the thin-film resistor module, and the result is connected to the comparator summing node. Thus the net current contribution to the node is a function of the digital switch inputs.

This page intentionally left blank

4.0 Gyro Reference Assembly*

4.1 Function

The Gyro Reference Assembly (GRA) measures (incremental) attitude of the reference block assembly with respect to inertial space and serves as the precision attitude reference between star sightings

4.2 Configuration

The GRA contains three single degree of freedom rate integrating gyros in analog torque rebalance loops. Digital to analog converters are used to provide pulse outputs. The PPCS 6-gyro configuration is obtained using two GRA's with the gyro input axes aligned normal to the surfaces of a dodecahedron, as shown in Figure 4-1

The GRA requires only prime power and clock synchronization signal. It has self contained clock, power supplies, torquing and digitizing electronics, and active temperature control. Independent electronics are provided for each gyro. A block diagram of one gyro channel is shown in Figure 4-2. Test provisions for gyro external torquing and torquer loop excitation for frequency response tests are provided.

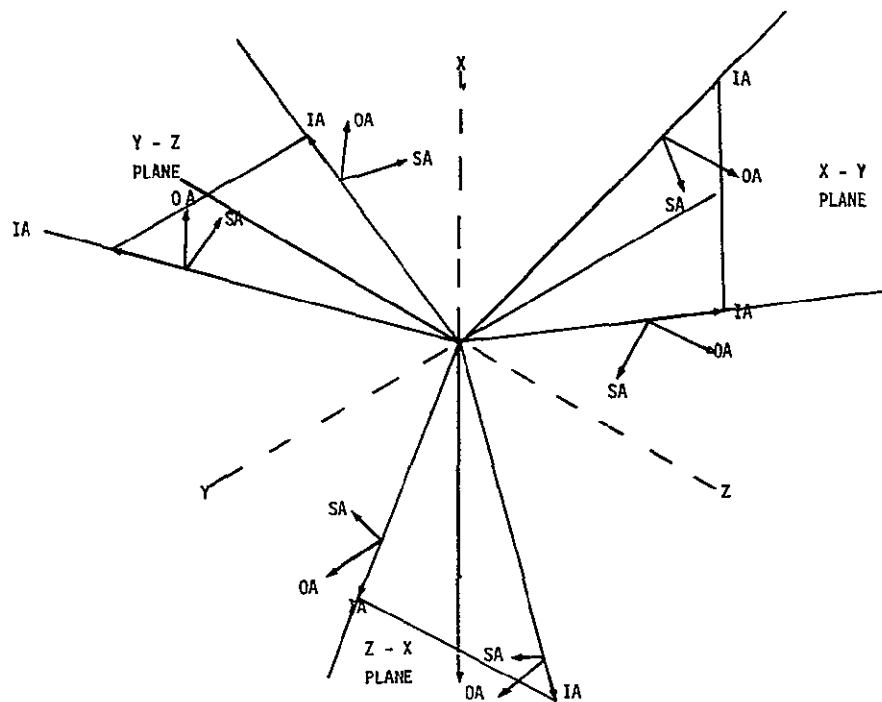


Figure 4-1 Gyro Input Axis Orientation With 6 Gyros

*This section is based on information provided by Nortronics

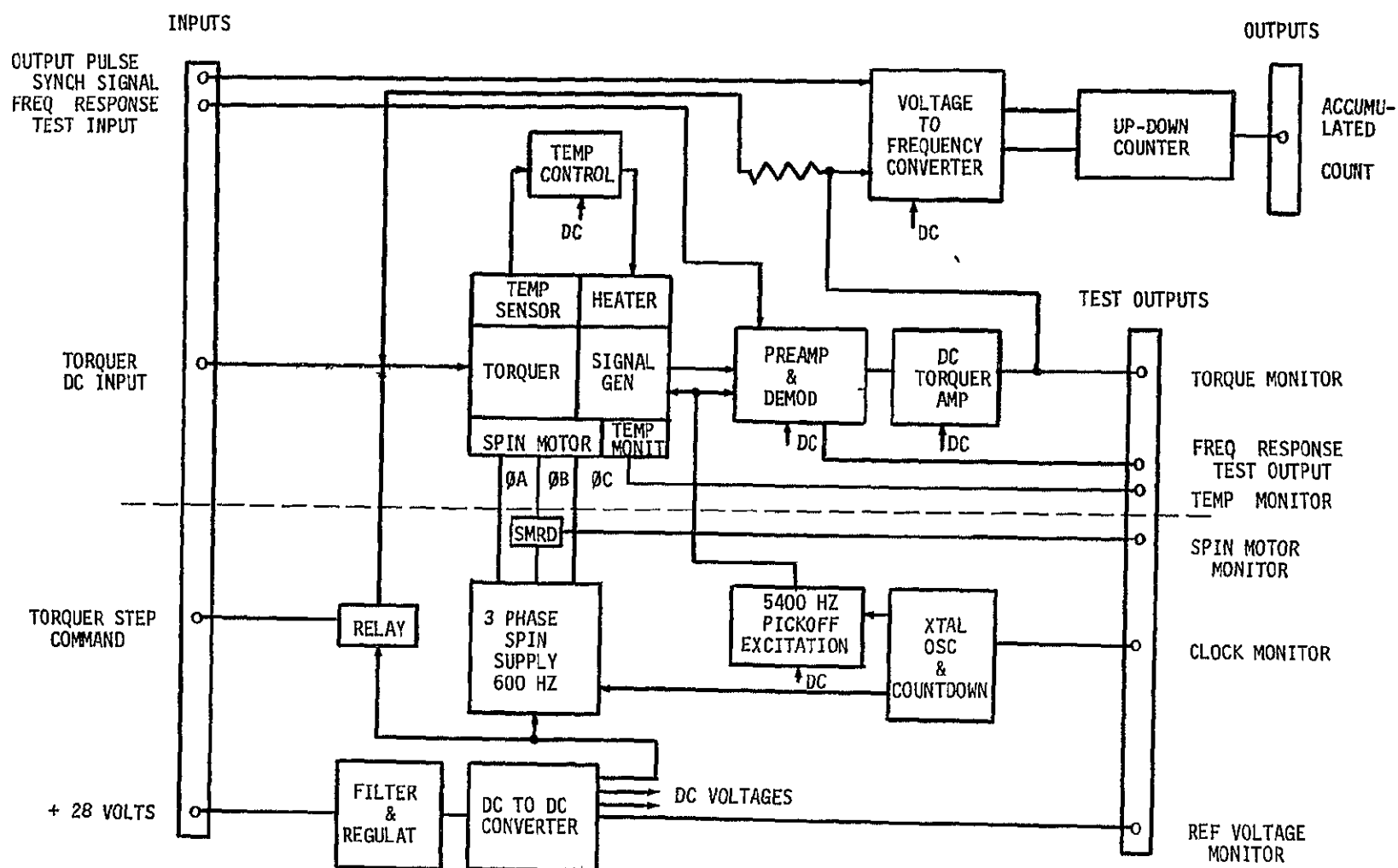


Figure 4-2 GRA Block Diagram

Figure 4-3 shows the GRA package. The three single degree of freedom gyros are mounted in close mechanical and thermal proximity on a common plate, attached to the mounting surface through a kinematic 3 point structure designed to minimize the effect of mounting surface temperature on the gyro alignment. The electronic components will be mounted to the base structure separate from the gyro, except for the temperature controller power transistor and critical electronic components. The package is not hermetically sealed. The weight of the GRA is 9 pounds, and the dimensions are 6 x 6 x 5.

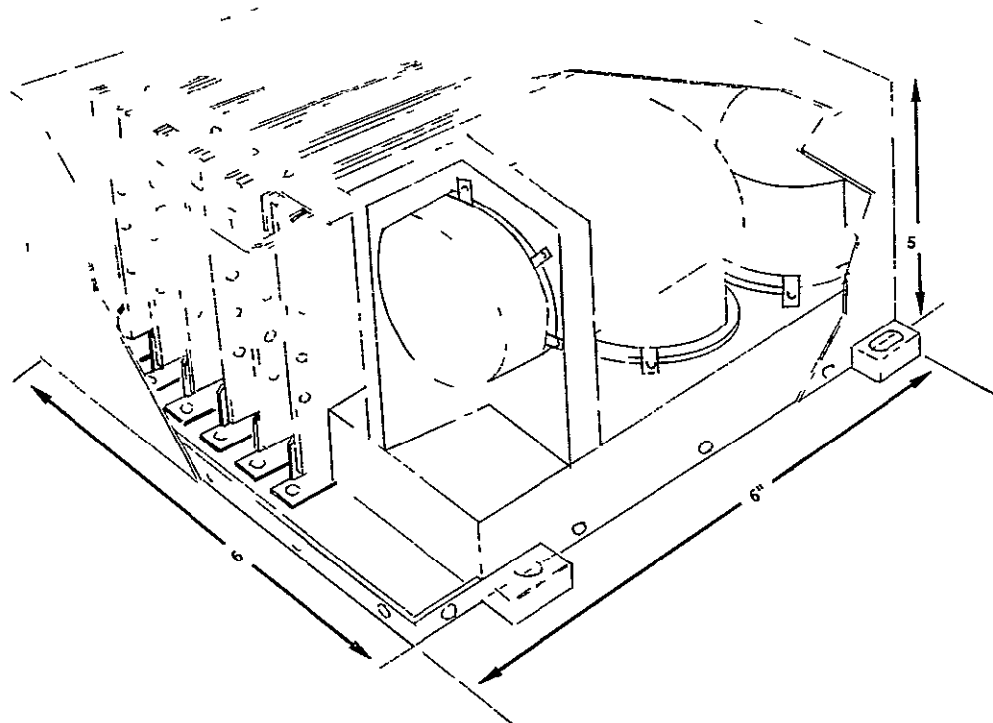


Figure 4-3 GRA Package

4.3 Operational Description

During launch and orbit insertion, the GRA is unpowered. In orbit, two modes of operation exist, heated for maximum stability and unheated for minimum power consumption. Normal PPCS operation is in the heated mode with 4 gyros running of the 6 available.

In the heated mode, active temperature control is used to maintain constant sensor temperatures. Maximum stability is achieved 30 minutes after application of heater power. Unheated, power consumption drops by about 50 watts.

and accuracy is degraded by a factor of approximately 2

The range of operation of the GRA is 15 degrees/second about all axes, with no limit on the total angle of rotation

The GRA outputs accumulated $\Delta\theta$ counts from an up-down counter controlled by the voltage to frequency converter. In the Digital Computer Assembly (DCA), these outputs are compensated for measured scale factor, drift, and misalignment and integrated into total inertial attitude angles. GRA drift is re-estimated and updated inflight at each star sighting. Scale factor and misalignment are calibrated in preflight tests.

4.4 Performance Characteristics

Physical

| | | |
|--------|---------------------|----------|
| Weight | 9 pounds | |
| Volume | 6 x 6 x 5 inches | |
| Power | Operating, Unheated | 15 watts |
| | Operating, Heated | 42 watts |

Gyro Torquer Loop Characteristics

| | |
|--------------|--------|
| Bandwidth | 10 hz |
| Gain Margin | 6 db |
| Phase Margin | 30 deg |

Attitude Measurement

| | |
|---------------------------------------|------------------------------|
| Rate Range | ± 15 deg/sec (each axis) |
| Angle Range | Unlimited |
| Scale Factor | 10 pulses/arc sec |
| Scale Factor Non-Linearity | 100 ppm |
| Scale Factor Stability (5 minutes) | 30 ppm (3σ) |
| Scale Factor Stability (Long Term) | 300 ppm |

Fixed Drift

| | |
|-----------------|---------------------------|
| Maximum Value | 1 deg/hr |
| Random (5 min) | 0.03 deg/hr (1σ) |
| 2 Day Stability | 0.5 deg/hr |
| Dynamic Drift | 0.036 deg/hr |

G Sensitive Drift

| | |
|---------------|-------------|
| Maximum Value | 10 deg/hr/g |
|---------------|-------------|

| | |
|-----------------|------------|
| 2 Day Stability | 2 deg/hr/g |
|-----------------|------------|

Input Axes Misalignment

| | |
|---------------|-----------|
| Maximum Value | 2 arc min |
|---------------|-----------|

| | |
|-----------------|------------|
| 2 Day Stability | 10 arc sec |
|-----------------|------------|

| | |
|---------------------|--------------|
| Long Term Stability | < 40 arc sec |
|---------------------|--------------|

Temperature Sensitivity

| | |
|-------------|---------------|
| Fixed Drift | 001 deg/hr/°C |
|-------------|---------------|

| | |
|--------------|-----------|
| Scale Factor | 30 ppm/°C |
|--------------|-----------|

| | |
|-----------|--------------|
| Alignment | 1 arc sec/°C |
|-----------|--------------|

Voltage Sensitivity

| | |
|-------------|---------------|
| Fixed Drift | 0005°/hr/volt |
|-------------|---------------|

| | |
|--------------|-------------|
| Scale Factor | 10 ppm/volt |
|--------------|-------------|

4 5 Design

The GRA Assembly design is based upon the Nortronics G1-K7G Gas Bearing Gyro. The expected performance is based upon TRW's and Nortronics testing of the G1-K7G Gyro and others of similar quality. Short term (5 min) random drifts were measured in a torque to balance mode (OA vertical) during the development of the Air Force's Minuteman Portable Alignment and Platform Mounted Gyrocompass and Nortronics development of the C5 Platform Gyro. Table 4-1 depicts the results of these gyrocompass tests.

TABLE 4-1 Short Term Gyro Random Drift Test Results

| <u>Manufacturer</u> | <u>Type</u> | <u>Random Drift (5 min integration) °/hr (1σ)</u> |
|---------------------|-------------|---|
| Nortronics | GIT | 0004 |
| MIT | 2FBG | 0014 |
| Sperry | Mod III* | 0010 |
| Sperry | Mod IV* | 0008 |
| Delco Electronics | 641* | 0009 |

| | | |
|--------------|--------|------|
| Kearfott | 2519 | 001 |
| Kearfott | 2590* | 0003 |
| Nortronics** | GI-K7G | 0004 |

* Gas Bearing

**Tested at Nortronics

4 5 1 Gyro Description

The GI-K7G Gyro design is an updated version of a long proven design. Approximately 350 units of an early version of this gyro and many of its proven components were produced, employing a ball-bearing wheel and a pivot/jewel output axis suspension. The present GI-K7G, of which 500 have been produced, employs a gas spin axis bearing and a taut wire output axis suspension. These improvements are the significant reasons for its superior performance.

The taut wire used for OA suspension eliminates the torque (drift) uncertainties due to the conventional pivot/jewel suspension. Any contact of the pivot with the jewel produce by misfloatation, fluid convection torques, float/case positional changes, or rates about OA will cause resultant frictional torques and drift uncertainties. The design features a Platinum Cobalt permanent magnet torquer which is free from reluctance effects, resulting in low 2nd order torque non-linearities.

The ferrotic gas bearing contributes to improved stability of the rotating wheel and is complemented with a beryllium float for a fully floated design. Elimination of the effects of physical wear in ball bearing greatly extend bearing life and reduces self generated vibration.

To reduce power, the wheel speed is reduced to 36,000 RPM for an angular momentum of 90,000 gm cm²/sec. The projected performance for this angular momentum, based on actual test data, shows the gyro is fully capable of meeting the performance requirements.

Gyro Model Equation

Since the gyros will be operating in a non-g environment, the error sources will be exclusively "strapdown" errors, those due to angular motion effects.

A model equation describing gyro response is

$$W_{IND} = W_{IN} + \theta_0 W_0 + \theta_S W_S + \Delta J_{OS} W_0 W_S \\ + J_0 \alpha_0 + W_B + W_R$$

where,

| | |
|-----------------|--|
| W_{ind} | is the indicated rate output signal |
| W_{IN} | is the actual input rate |
| W_B | is the sum of all non-g sensitive steady state drift effects |
| ϕ_0 | is the output axis rate sensitivity (IA about SA misalignment) |
| ϕ_S | is the spin axis rate sensitivity (IA about OA misalignment) |
| ΔJ_{OS} | anisoinertia coefficient at low frequencies up to approximately 3 Hz |
| J_0 | effective moment of inertia about the gyro output axis |
| W_R | residual errors not accountable under other model terms |
| W_0, W_S | rates about the gyro output and spin axes |
| α_0 | angular acceleration about the gyro output axes |

Coning errors do not originate at the gyro, but are correctable at the computer
Cross coupling errors are considered negligible in the low rate environment

Three-Phase Gyro Wheel Supply (Figure 4-4)

The 3-phase gyro wheel supply consists of three major circuit components, a switching regulator, square wave supply, and a start/run mode control logic. The gyro wheel excitation is generated by applying a regulated DC voltage to a 2-phase (120° apart) DC/AC square wave supply. The resulting 2-phase waveforms are transformer coupled and wired in a standard open-delta 3-phase configuration. In the interest of minimizing the starting power, a dual mode of

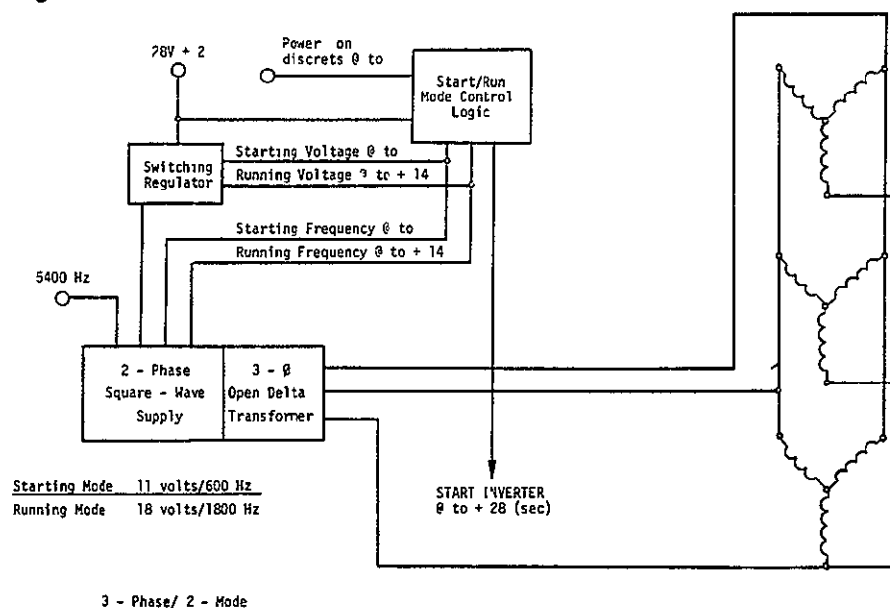


Figure 4 4 Gyro Wheel Supply

operation is incorporated in the wheel supply design. The starting mode provides the gyro wheels with 11 volts RMS at 600 Hz for the first 14 seconds of operation. The running mode is initiated after the initial 14 second period. In this mode, the gyros are operated at 18 volts RMS at 1800 Hz wheel excitation. The mode control signals are internally generated by a run/start mode control module. A discrete external command pulse initiates the mode control logic sequence.

Inverter and DC Supply (Figure 4-5)

The inverter and DC supply converts the primary 28 volt input power into the necessary internal power supplies required to operate the analog and digital circuitry. The inverter is commanded "ON" 28 seconds after the initiation of the external package "ON" discrete, this time delay allows the inverter power surge to be non-coincident with the gyro wheel-power surges. The inverter timing is synchronous with the system clock.

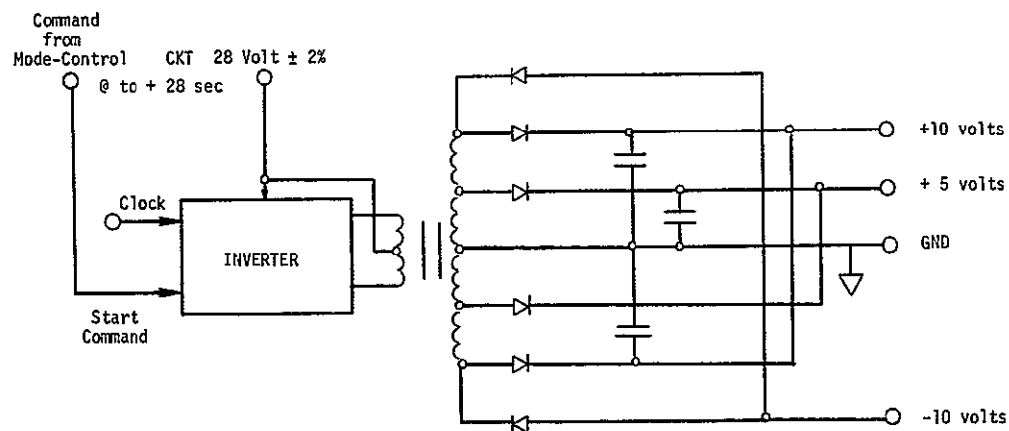


Figure 4-5 Inverter & DC Supply

AC Amplifier and Demodulator (Figure 4-6)

The gyro input axis rate is sensed by the gyro and a suppressed - carrier modulated signal is developed which is proportional to the displacement of the gyro float from the electrical null. This AC signal enters into the AC amplifier module through the proper matching impedance of the first-stage operational amplifier. The amplified gyro error signal then passes on to the full-wave demodulator circuit.

In the demodulator circuit, two MOSFET's are used as a shunt chopper circuit. In this configuration, a single demodulator reference-drive signal is required to bias on and off the electronic switches. The chopper transistors convert the error signal into two half wave rectified signals. These signals are then applied differentially to the operational amplifier where they appear at the output as a full wave rectified signal. The rectified signal then passes to the filter network which attenuates the higher carrier - associated harmonics and transmits the lower frequency gyro error information.

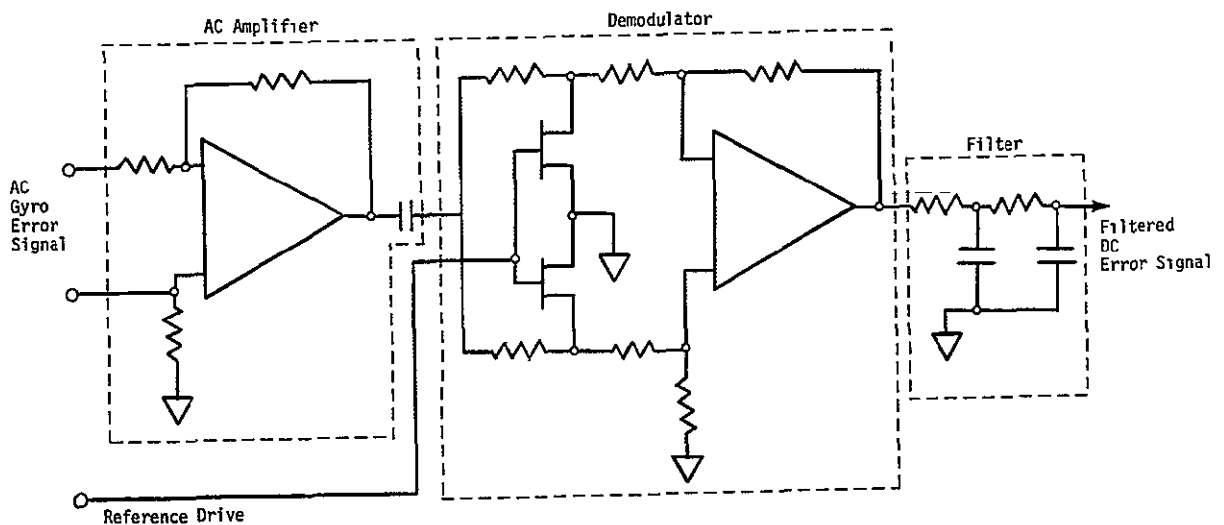


Figure 4-6 AC Amplifier and Demodulator

Temperature Controller (Figure 4-7)

The temperature controller controls a 70 watt heater element for warmup, and a 20 watt heater for normal mode which is located within the gyro cluster. A temperature sensor is also located within the sensor assembly. The circuit is mechanized as a pulse width controller. The temperature sensor change is DC amplified and is compared with a reference sawtooth waveform. This is differentially summed into a threshold detector which generates the pulse output whose width varies as the sensor resistance varies. An enable/disable command capability is also incorporated into the design.

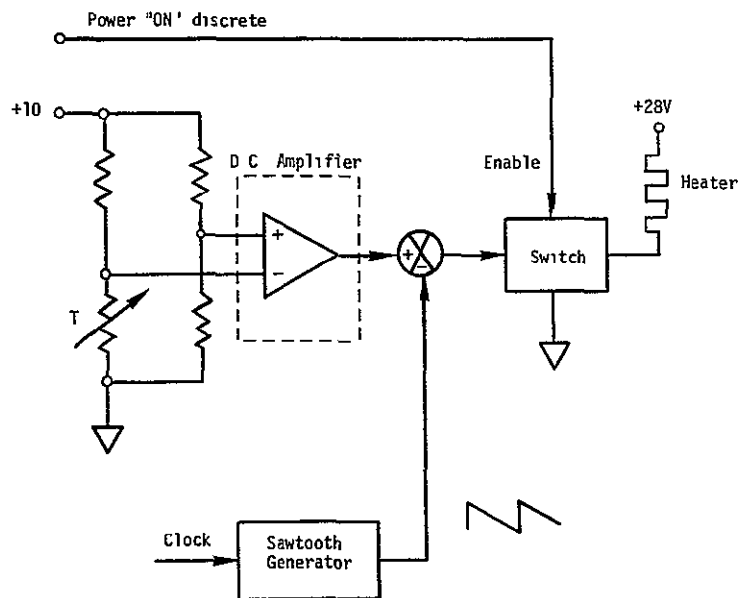


Figure 4-7 Temperature Controller

Analog Torque to Balance Electronics (Figure 4-8)

Torquing the gyro float to an electrical-null is accomplished by summing the compensated demodulated error signal into a current amplifier which drives a proportional current into the gyro torquer. An ultra-precision current-sampling resistor is placed in series with the torquer for read-out purposes. A precision readout amplifier is used to buffer the sampling-resistor voltage, and provide a scale factor adjust capability.

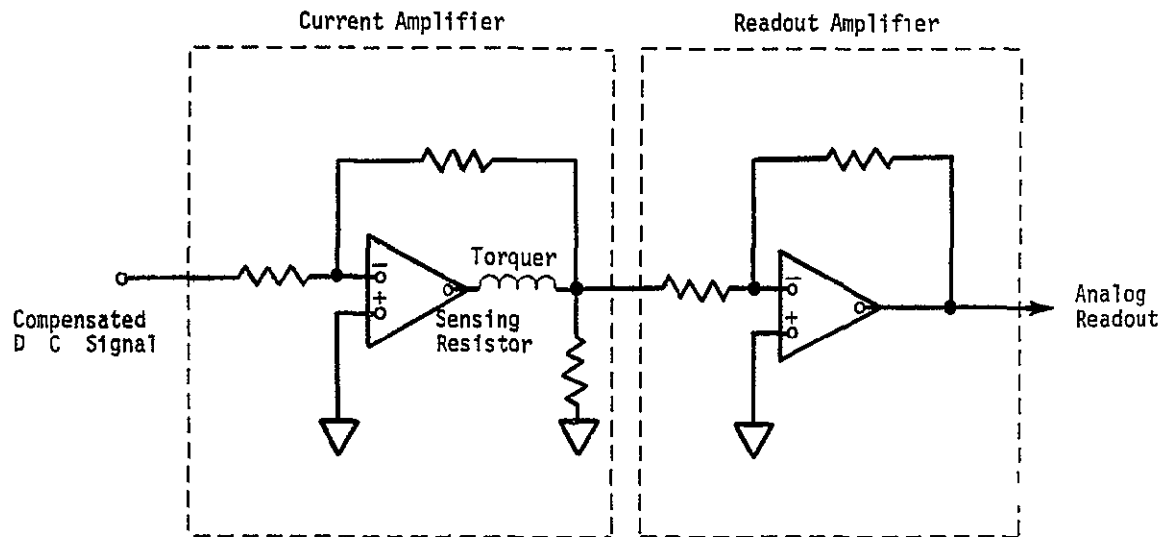


Figure 4-8 Rebalance Electronics

Voltage-to-Frequency Converter (VFC) (Figure 4-9)

A Voltage-to-Frequency Converter (VFC) is utilized to accomplish the analog-to-digital conversion of the output rate signal. A block diagram of the VFC is shown in Figure 4-9. A precision integrator of the operational amplifier type serves as the input circuit of the VFC. The integrator output is impressed upon a pair of level detectors connected in parallel. Their individual outputs are either high or zero depending on their input condition. One level detector is high when the integrator output is greater than a reference threshold of +70 millivolts, otherwise, its output is zero. Similarly, the other level detector is high when the integrator output is less than -70 millivolts, and zero otherwise. When either level is high, the logic connected to the level detector output commands a precision current source and a current switch to provide a rebalance pulse of current to the input of the integrator. The polarity of the applied pulse is determined by the sign of the threshold that was exceeded, and the pulse start time and length are controlled by the clock signal. The result is a pulse-on-demand feedback loop which provides constant area current pulses of the proper sign, in synchronism with the

clock frequency, which tends to hold the integrator output within the threshold values. The VFC output consists of two pulse trains indicating that positive or negative current pulses have occurred. Each output pulse represents a fixed amount of rebalance charge applied to lower the voltage across the integrating capacitor. The result is that the algebraic sum of the two pulse trains is proportional to the VFC input volt-seconds, which, in turn, is proportional to the gyro input angle rotation.

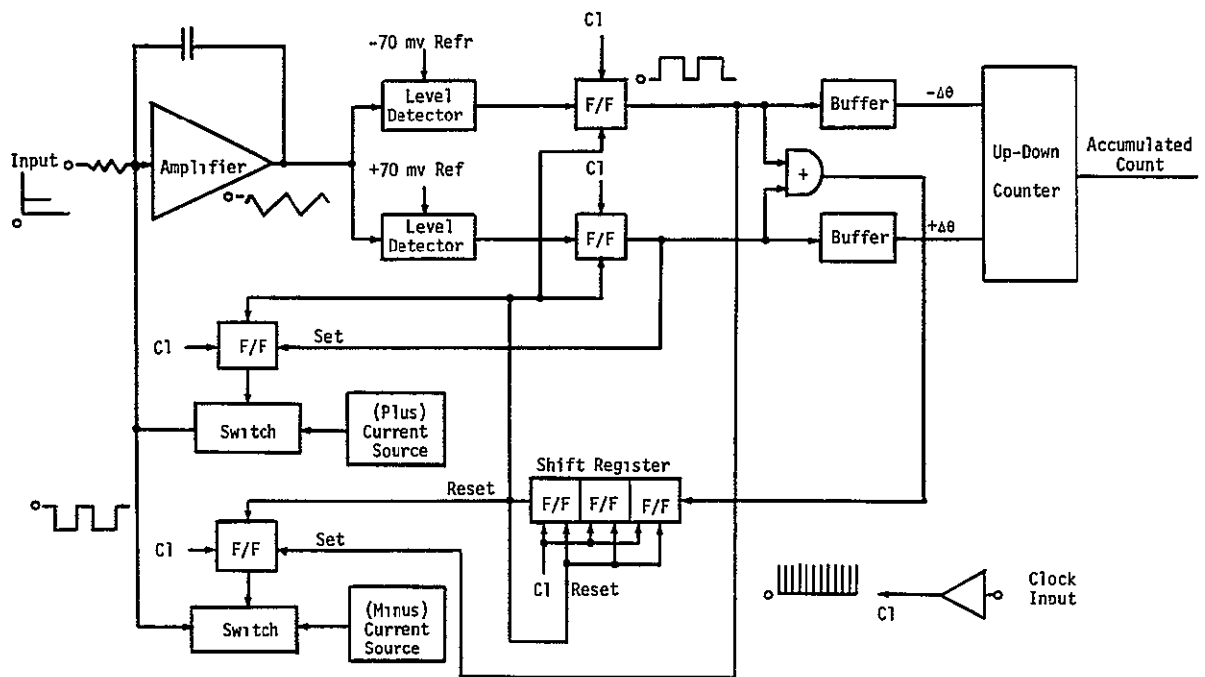


Figure 4-9 Voltage-To-Frequency (VFC) Block Diagram

Scale Factor Compensation

The scale factor temperature sensitivity is adjusted through thermistor network compensation at the rebalance loop scaling resistor. The thermistor is mounted directly on the gyros in close proximity to the gyro torquers. The scale factor sensitivity is modeled from measurements made at various temperatures. At $1^\circ/\text{sec}$, the scale factor change over the 50°C range amounts to $50 \text{ ppm}/^\circ\text{C} \times 50^\circ\text{C} \times 3600^\circ/\text{hr} = 9^\circ/\text{hr}$, indicating the test temperature resolution will be more than adequate.

5 0 Reference Block Assembly

5 1 Function

The Reference Block Assembly (RBA) serves as a structural platform for mounting the Star Tracker Assemblies, the Gyro Reference Assemblies, and the Attitude Transfer Assemblies. It incorporates a thermal control system for maintaining low thermal gradients and resultant structural deformations.

5 2 Configuration

Figure 5-1 is a layout drawing of the RBA showing its position within an 8 0 foot diameter spacecraft. Its position is established by the requirement that the Star Tracker field of view, in elevation, be 90° to 180° away from local vertical.

The RBA is a structure which is shaped like an equilateral triangle and is supported at each apex. The six Attitude Transfer Assemblies are arranged in the form of a hexagon centered within the triangle on the Earth-facing side, and the Gyro Reference Assemblies are located on the opposite side at the geometrical center of the RBA. The Star Tracker Assemblies are overhung from one leg of the triangle in order to minimize the size of the window required in the spacecraft. The RBA is made of 6061 aluminum and is basically a box structure, 10 inches deep with 20 inch thick aluminum plates on each side.

Thermal control is achieved by mounting each heat-generating component on an aluminum plate which is isolated from the RBA by means of insulating standoffs. Heat is carried away from the plates by means of heat pipes and rejected to a large radiator. This radiator may be located directly above the RBA and may reject its heat to space. Isolation from the spacecraft is achieved by wrapping the entire RBA with insulation blankets.

5 3 Operational Description

The RBA and its thermal control system are entirely passive. Its operational performance requirements are simply to maintain the required alignment between components. It achieves this goal, in part, by rejecting component-generated heat through heat pipes.

5 4 Performance Characteristics

| | |
|--|----------|
| Maximum Vibration lead transmitted to each component | 10 0 g's |
|--|----------|

| | |
|--|-----------------------------|
| Maximum distortion between any two components due to thermal effects | 1 5 $\overline{\text{sec}}$ |
|--|-----------------------------|

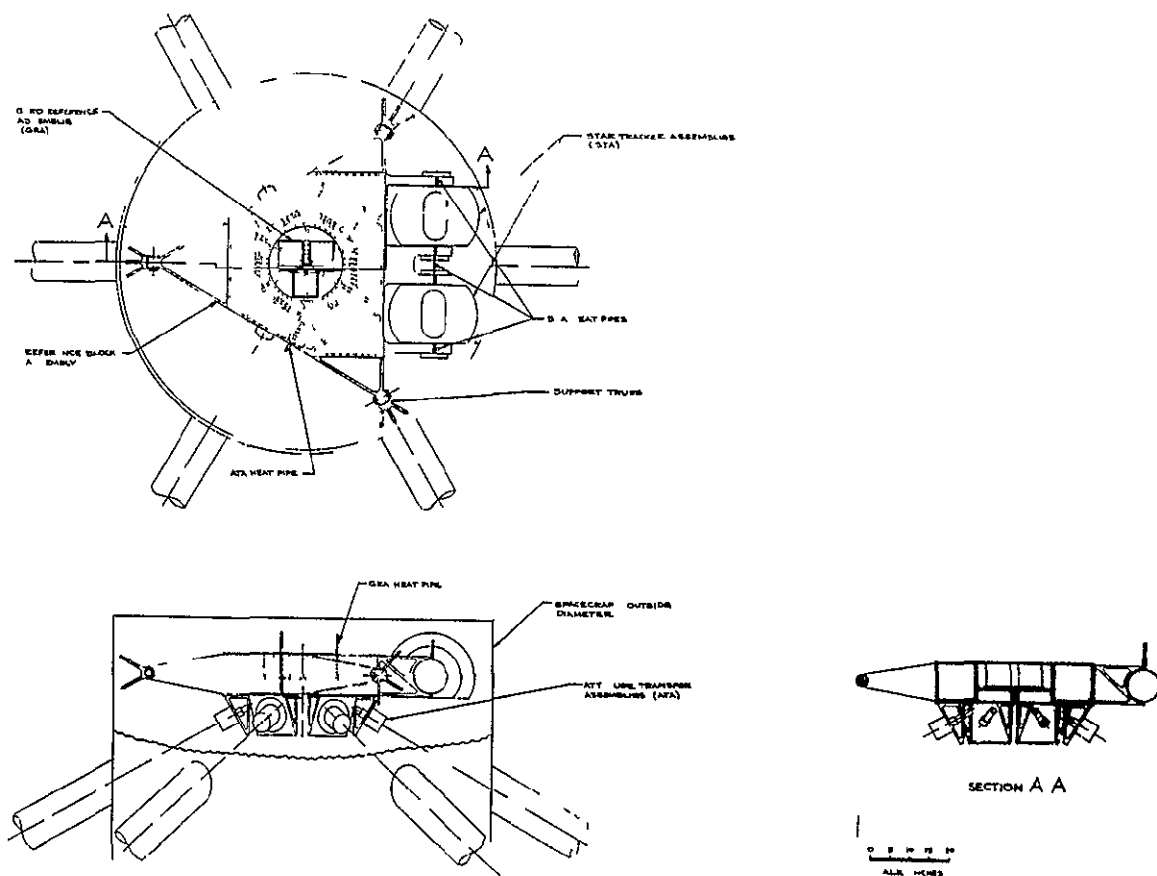


Figure 5-1 Reference Block Assembly Layout

mounting surfaces, four of each unit. It is proposed that the radiator be located directly above the RBA, at the space-facing side of the spacecraft. Approximately 51 square feet of radiating area are required. Insulation from the spacecraft is achieved by wrapping the entire RBA with insulation blankets.

6 0 ATTITUDE TRANSFER ASSEMBLY*

6 1 Function

The Attitude Transfer Assembly (ATA) measures the attitude (3 axis, z, y twist) of the remote Experiment Gimbal Assembly base relative to a set of axes defined at the ATA mounting

6 2 Configuration

The ATA consists of a dual-axis tracking autocollimator cooperating with a plane mirror for measuring z, y attitude and a single-axis instrument used with two dihedral (Porro) reflectors for measuring twist Figure 6-1 shows the optical arrangement The y, z autocollimator uses a collimated light beam reflected from a mirror attached to the gimbal base to produce a two axis error signal The collimated beam is deflected by a servo controller such that the beam remains perpendicular to the mirror The twist system uses a similar collimated beam with two Porro reflectors, one at the boom

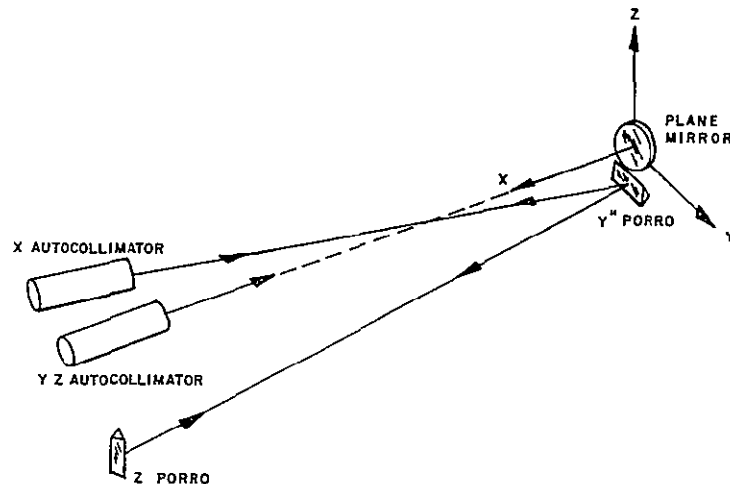


FIGURE 6-1 Attitude Transfer Optical System Diagram

end and one at the autocollimator end The twist measurement is obtained by projecting a collimated beam to the Porro reflector at the far end of the boom This reflector is arranged with its roof parallel to the y axis The beam is reflected to the vertical Porro reflector at the near end from where it retraces its path back to the autocollimator Rotation of the

* This section is based upon the Barnes Engineering Company final report, Reference 6

remote reflector about x produces a vertical component of beam movement sensed in the autocollimator which is $(4 \sin \theta) \Delta \phi_x$, where θ is the angle between the autocollimator and the boom center line and $\Delta \phi_x$ is rotation angle about x. Rotation about y produces no vertical component. Rotation about z is cancelled by the reflection of the vertical reflector. Figure 6-2 shows the equipment arrangement. The two autocollimators and one Porro reflector are mounted on a plate which is designed to attach to the Reference Block Assembly. The remote mirror and Porro reflector is mounted on the base of the Experiment Gimbal Assembly. Each autocollimator is about 10" long and has a maximum diameter of 4.7 inches. Each weighs 8.93 pounds. The remote Porro reflector is 4.5" x 4.5" and weighs 2.6 pounds. The mirror is 4.5 inches in diameter and weighs 1.4 pounds. The small Porro reflector weighs 0.9 pounds. The mounting plate weighs 5.1 pounds. The total 3 axis system weighs 27.9 pounds and consumes an average of 7.5 watts of power. A functional block diagram of the y, z autocollimator is shown in Figure 6-3. The light source is a pulsed Gallium Arsenide diode which emits at 8900Å. A source reticle and field lens images the source on a collimating lens to produce a collimated beam. This beam then passes through two pairs of optical wedges, each having the function of compensating and measuring one mode of rotation. Initially, the wedges in each pair are opposed and the deviation of the first is cancelled by the second. The collimated beam proceeds without deviation and is reflected by the mirror (or Porro for the twist system) and returns to the autocollimator where it is imaged on separate detector reticles. The reticles have an opaque area matching the source reticle so that, for no mirror deviation, the return image is blocked by the opaque area and no error signal is produced. Mirror rotation causes the image to move off center and produces an error signal which is detected and used to drive the wedges. They rotate in opposite directions and thus each pair produces beam deflection in only one axis. The wedges are driven until the error signal is nulled - the rotation required is a measure of the mirror angular motion. This rotation is measured by the resolver. The wedges are driven by a stepper motor and gear train. The resolver is directly coupled to the wedges to avoid gear errors. Since a several step deadband is used in the wedge servos, the analog error signal is also provided as an output. The resolver signal is combined with the analog error signal to give the measurement. The stepper motor drive rate is sufficient to null errors at a 200 arc sec per second rate. The twist system is similar, except that the second wedge set is slaved to the x, z compensation wedges in the y, z autocollimator to remove a cross coupling error.

6.3 Operational Description

During launch and initial spacecraft orientation, the ATA is quiescent. The payload booms are deployed and locked into position. The ATA is turned on with

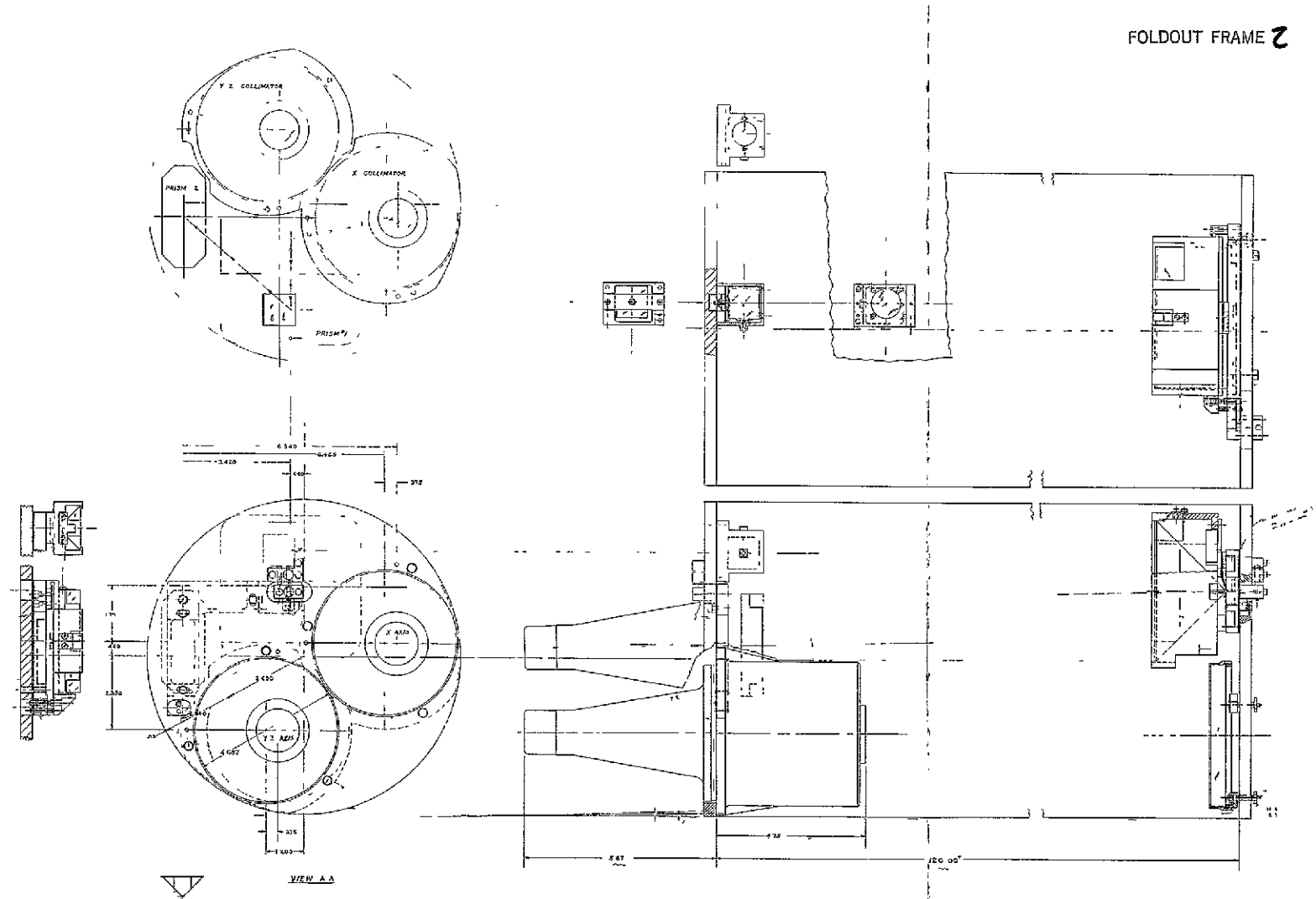


FIGURE 6-2 Mechanical System Diagram

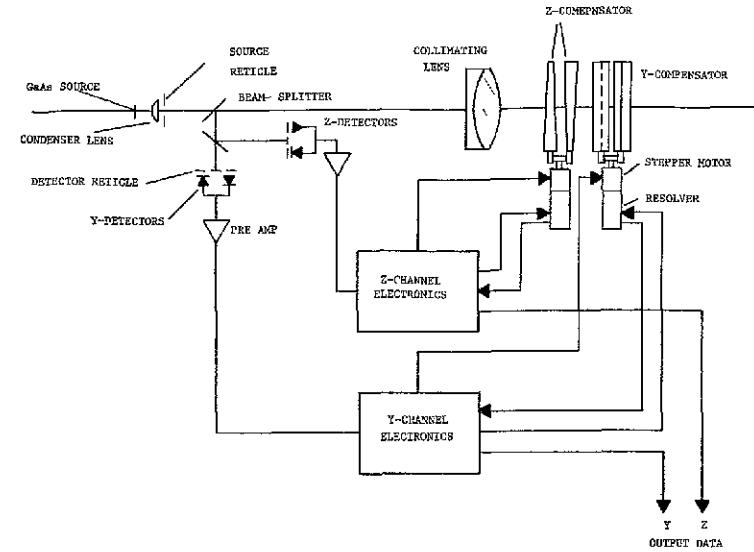


FIGURE 6-3 ATA Functional Block Diagram

the other PPCS assemblies. An acquisition phase to allow the autocollimators to acquire the return light beam follows. This is done by commanding the stepper motors (from the computer) to drive the wedges over their entire operating range. When the return beam is sensed, the autocollimator locks out the computer drive and enters normal mode. The autocollimator tracks automatically any motions of the return beam and provides 3 axis output signals to the computer.

During PPCS calibration, static errors in the ATA will be determined and appropriate compensation made. The ATA incorporates the capability to calibrate the analog error signal. Under computer control, a predetermined number of motor steps is commanded, thus displacing the wedges from null. The computer can then sample the off-null autocollimator outputs and develop a scale factor compensation.

6.4 Performance Characteristics

Attitude Transfer Assembly performance characteristics are summarized in Table 6-1.

TABLE 6-1 Performance Characteristics

| | | |
|---------------------------------------|---|------|
| Type Measurement | Nulling Autocollimator | |
| Range | > 10 ft | |
| Angular Measurement Range | $\pm 0.5^\circ$ Rotation (3 Axis) combined with ± 0.5 in translation of remote end | |
| Tracking Rate | 200 Arc sec per sec | |
| Focal Length | 12.7 cm | |
| Aperture | 3.2 cm | |
| Weight (Total) | 27.9 | |
| Power (AVE) | 7.5 watts | |
| Accuracy (Arc Sec, 1σ) | y-z | x |
| Repeatable Mechanical & Elec Errors | | |
| Orthogonality | 0.17 | - |
| Alignment | 0.10 | 0.07 |
| z Follower Align | - | 0.33 |
| Resolver Nonlinearity | 0.04 | 0.04 |
| Resolver Alignment | 0.10 | 0.10 |
| Cross Coupling | 0.10 | 0.80 |
| Random Mechanical & Electrical Errors | | |
| Noise | 0.01 | 0.03 |
| Mirror Error | 0.10 | - |
| Prism Error - Large | - | 2.0 |
| - Small | - | 0.5 |
| Stability Errors | | |
| Detector Null | 0.01 | 0.08 |
| Thermal Bending | 0.01 | 0.23 |
| Analog Signal Error | 0.08 | 0.08 |

6.5 Design

Figure 6-4 shows a cross section of the autocollimator. The light source and detectors are mounted in a tapered beryllium housing which is designed to provide a stiff, stable alignment of the optics. The housing is isolated thermally from the wedge drive assembly by a fused ceramic layer at the five mounting pads. The mounting bolts for the housing are also insulated with ceramic washers. A thick cross section near the mounting interface is included to minimize thermal gradients in the housing. The collimating lens

is mounted in a screw-in subassembly which is locked into place by the set-screw shown

Bearings

The optical wedges and their drive/readout system are mounted in an aluminum housing. The counter-rotating wedges are each supported by a pair of pre-loaded angular contact bearings. Table 6-2 summarizes bearing characteristics.

TABLE 6-2 ATA Bearing Characteristics

| | |
|-----------------|-----------------------|
| Manufacturer | Split Ball Bearing Co |
| Number | 3TAL26-30U DP |
| Preload | 25 lbs |
| Contact Angle | 20 ° |
| Starting Torque | 1.07-in |
| Bore | 1.675" |
| OD | 1.875" |
| Width | 0.156" |

Bearing lubrication is Andoc C grease, which is a sodium-based grease, manufactured by ESSO. Labyrinth seals are used to inhibit lubrication loss.

Resolver

The rotor of a hollow shaft multispeed resolver is mounted to one wedge of each wedge-pair. To maintain close control of resolver stator-rotor concentricity, the resolver is mounted prior to finish machining the surfaces mounted to the bearings. By selective mounting of the bearings so that their runout opposes the residual eccentricity of the resolver motor and stator mounts, the required resolver concentricity is achieved. Resolver characteristics are summarized in Table 6-3.

TABLE 6-3 ATA Resolver Characteristics

| | |
|--------------|-------------------------|
| Manufacturer | Reeves Instrument Co |
| Part No | DPX-33D-001 |
| Speeds | 16/1 Dual |
| Excitation | 1024 Hz, 5 v RMS, Sine |
| Accuracy | ± 15 arc sec (16 speed) |

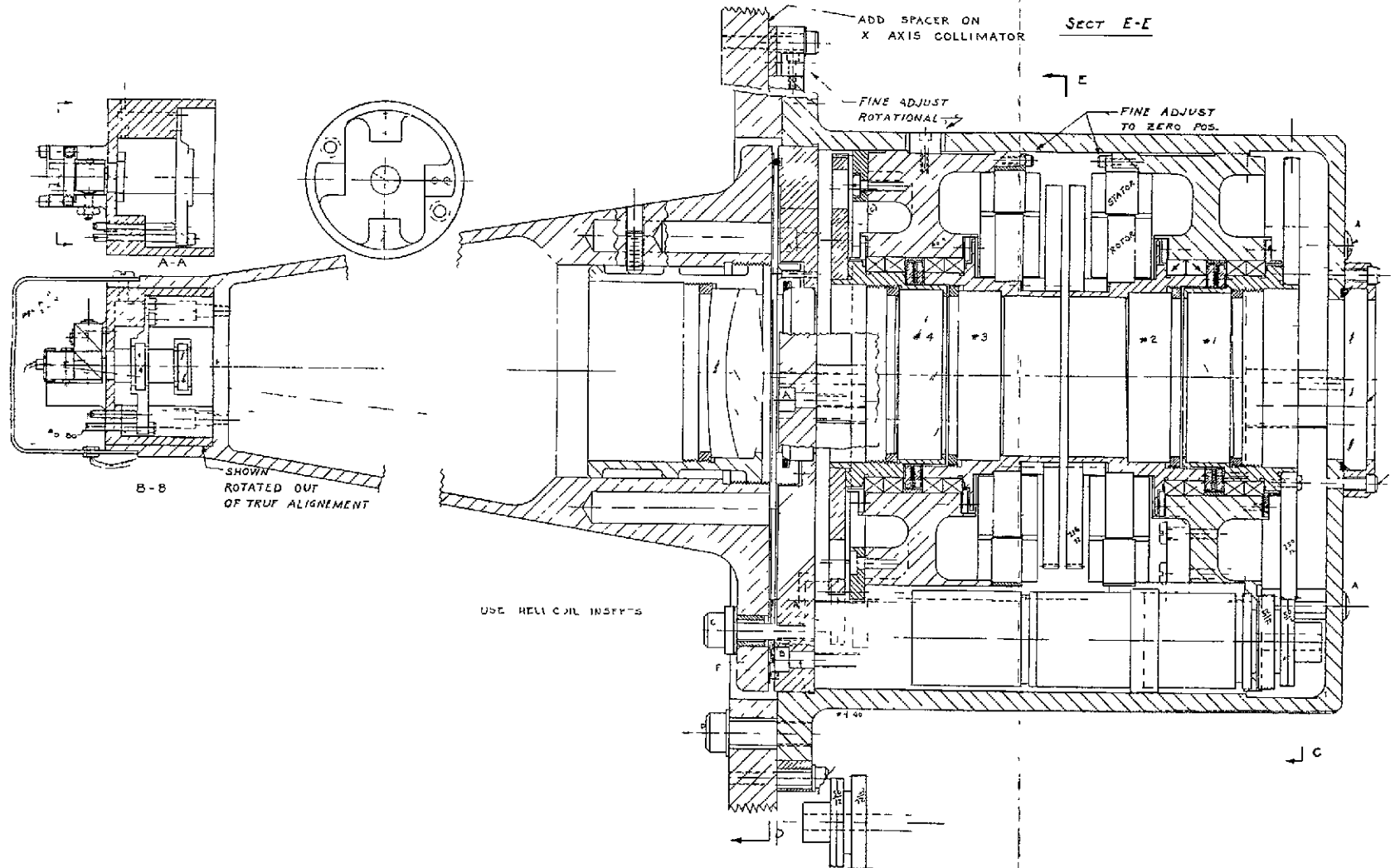


FIGURE 6-4 Autocollimators Cross Section

Stepper Motor and Gearhead

The wedges are driven by a stepper motor - gearhead combination. A size 8, 45° degree per step, permanent magnet stepper motor is used. The gear reduction of 2700:1 is provided by two anti-backlash gearheads specially designed by Sterling Instrument. Stepper motor characteristics are summarized in Table 6-4.

TABLE 6-4 ATA Stepper Motor Characteristics

| | |
|-------------------------|--------------------------|
| Manufacturer | Computer Devices Corp |
| Model No | 08M-01 |
| Type | Size 8, Permanent Magnet |
| Stepping Angle | 45° |
| Max Step Rate (No Load) | 700 step/sec |
| Stall Torque | 1 in-oz |
| Rotor Inertia | 0.3 gm-cm ² |
| Operating Voltage | 28 vdc |
| Input Power (Peak) | 13.7 watts |

Optics

Figure 6-5 shows an exploded view of the optics. The source is a Gallium Arsenide diode which emits at 0.9 micrometers with a half-spectral width of 0.04 micrometers. It radiates over a circular area 0.015 in diameter.

The emitting area is covered by the manufacturer with a lens in optical contact with the emitting area. This lens is made of Epon 838, an organic material, and its purpose is to channel the wide-angle emission of the source into a narrow lobe. Since this lens is not precisely controlled in manufacture, however, there is a large variation in lens characteristics.

Barnes Engineering Company has developed a construction which replaces this lens with a closely defined optical subsystem designed to image the source area onto the aperture stop at the objective lens. The Epon lens is removed with a diamond saw and a glass lens is cemented in its place using the same Epon material. This matching of material reduces reflection loss and provides a solid bond between source and lens.

The lens is mounted close behind the source reticle, which defines the angular spread of the beam in collimated space. The source reticle is cemented to a beam-splitting cube cluster. This cluster has three surfaces which are

is given by

$$d = t(n-1) \tan l^\circ/n$$

For glass of index $n = 1.509$, the shift

$$\begin{aligned} d &= 0.060 \times 0.509 \times 0.0175/1.509 \\ &= 0.000354 \end{aligned}$$

For a focal length of 5 inches, the angular change of the collimated beam $= 0.00007 \text{ rad} \approx 14.6 \text{ arc-sec}$. Thus a reduction of 240 is obtained which makes it entirely feasible to adjust the pointing direction with a precision of an arc-second without difficulty. The plates are adjusted by push-pull screws, and the mechanism is designed with emphasis on stability after the plates are adjusted and locked.

The collimating (objective) lens has been designed to correct spherical aberration. The small chromatic aberration represented by the narrow spectral band of the source is not fully corrected, because to correct such a narrow band is actually more difficult than a normal blue-red span.

One of the favorable characteristics of this tracking autocollimator is that the collimator itself is always operating under uniform conditions. The image is held on the optical axis, and the aperture is always filled with light from the returning beam. This is, there is no vignetting or asymmetry to introduce off-axis or variable aperture effects.

Consideration was given to making the wedges achromatic. With single wedges, the angular dispersion represented by the 40 nm spectral half-width of the source is $\pm 1.15 \text{ arc-sec}$. If the source were constant in spectral character with time and temperature this would be of no concern, especially since the silicon detectors have nearly flat response in the wavelength region of the source emission.

A change of 15° C produces two effects which are related to wavelength. The spectral emission of the source changes by 4.2 nm, and from the dispersion of the glass used for the wedges (Borosilicate Schott BK-7) the change in index due to wavelength change is -6.5×10^{-5} . This produces a change in deviation of the pair of wedges of -0.23 arc-sec when set to produce 1800 arc-sec deviation.

In addition to this effect is the change of index of the glass due to temperature. The index of refraction of the glass increases with temperature enough to produce a change in deviation of $+0.13 \text{ arc-sec}$ for a $+15^\circ \text{ C}$ temperature change. Therefore the net effect is a mere 0.10 arc-sec for a combination of maximum temperature excursion and maximum deviation.

Windows close both ends of the wedge-drive housing for protection during pre-launch and also to reduce the rate of evaporation of the lubricant. Although the unit is not hermetically sealed, all transmitting air-glass surfaces are coated with a high-efficiency anti-reflection coating, with reflection loss not to exceed 0.5 per cent per surface. All mirror surfaces are coated with evaporated gold and over-coated with silicon monoxide for protection. The reason for using gold instead of aluminum is the fact that the latter material has a substantial absorption dip in the spectral region around $0.85 \mu\text{m}$. The system transmittance would suffer a loss of approximately 15 per cent per reflecting surface using aluminum, whereas gold has a reflectance of around 98 per cent in the same region.

Detector

The detector for each channel is comprised of two silicon photovoltaic sensors connected so as to be electrically in parallel and to respond with opposite phases to incident light from the optical system. A minimum output is provided when the optical system is at null. The impedance of the detector is approximately 2 megohms and is operated unbiased to provide maximum stability. The detector is tested for responsivity at 0.9 micron, which is the wavelength of peak emission of the GaAs infrared source, and selected for a 5% match. The detectors will be N on P Silicon based on experience reported by Philco-Ford, which shows this type to be substantially more resistant to radiation damage in space environment than the more commonly used P on N.

The x channel will be operated with a chop frequency of 819 Hz. The y and z channels will be operated at a frequency of 1638 Hz. Separate frequencies for each channel are used in order to minimize cross-coupling errors.

Electronics

Figure 6-6 shows a block diagram of the ATA electronics. An external clock is counted down, amplified, and used to drive the light-emitting-diode (LED). The return signal at the detector develops an error signal which is amplified, demodulated, and used to drive the stepper motors so as to null the error. Excitation is provided to multispeed resolvers, whose outputs are used to measure the wedge position. The analog error signal is also provided as an output.

Preamplifier

A schematic of the video channel is shown in Figure 6-7. The detector is followed by a low-noise FET input pre-amplifier. The circuit uses discrete components in a feedback configuration providing a high input impedance,

SYSTEM DIAGRAM

FOLDOUT FRAME 2

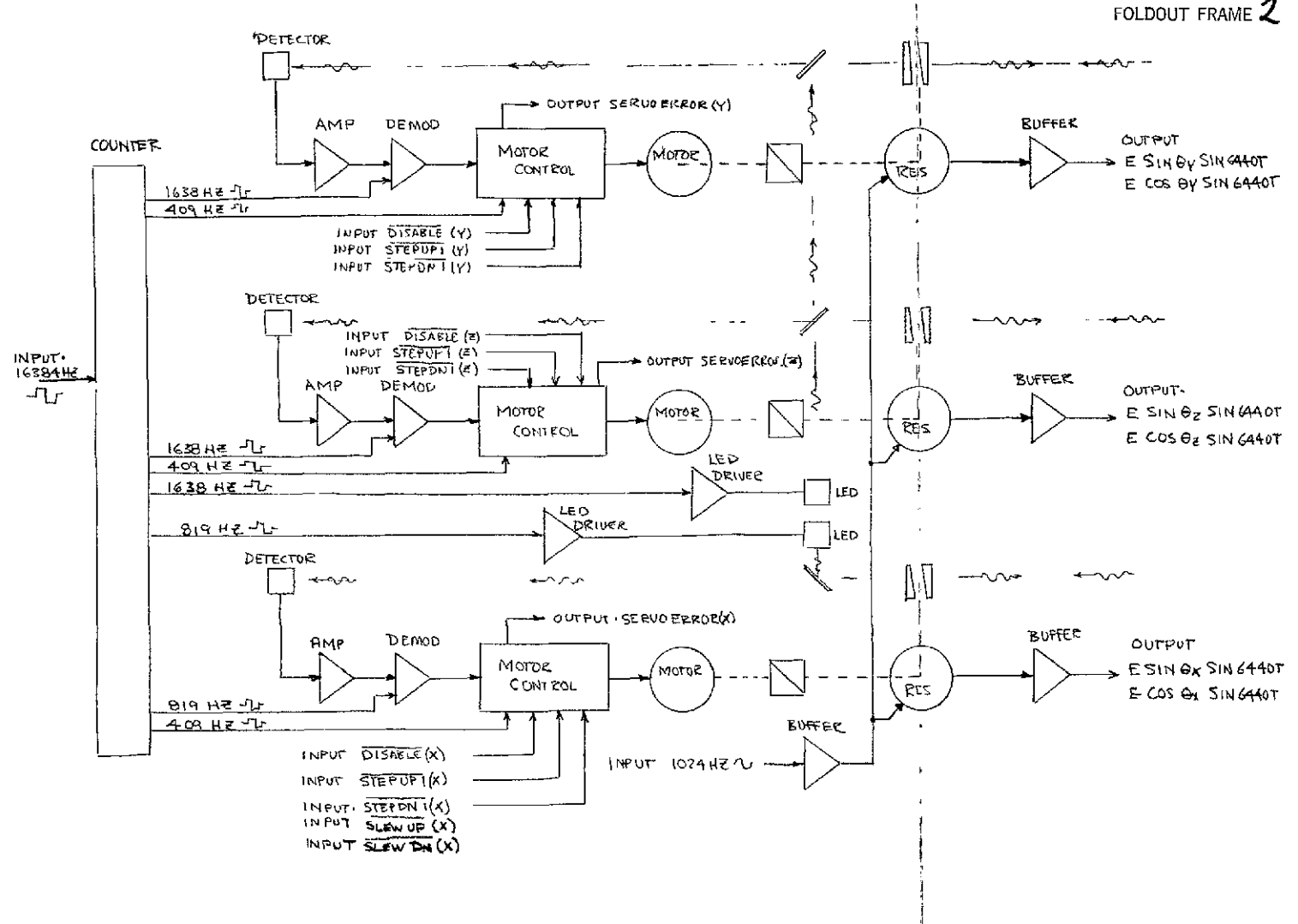


FIGURE 6-6 ATA Electronics Block Diagram

low output impedance, and stability of gain. Effects of component variations due to tolerance or environmental changes are minimized. The circuit has a high open loop gain and a closed loop gain of 20. The input signal level to the preamplifier in the x channel for a one-second rotation of the mirror is 50 microvolts. This signal level out of the preamplifier is therefore

$$50 \times 10^{-6} \text{v} \times 20 = 1 \times 10^{-3} \text{v}$$

or 1 millivolt

Post Amplifier

The signal from the preamplifier is coupled to the post amplifier to provide additional gain for the signal before it is applied to the demodulator.

The post amplifier includes an integrated circuit operational amplifier with high open loop gain and a closed loop gain of 200. This provides a signal level at the output of $1.0 \times 10^{-3} \times 200 = 0.2$ volts. The post amplifier will be ac coupled at the input and provide minimum distortion of the signal waveforms. The upper frequency break point is 8 KHz.

Demodulator

The output of the post amplifier is a square wave signal with an amplitude and phase characteristic which corresponds to the magnitude and direction of rotation of the mirror away from null. The signal is applied to the demodulator which converts the directional information to a positive or negative level and magnitude information to an output amplitude.

The demodulating waveform is a square wave of the same frequency as the carrier and is synchronous with the carrier. The circuit uses solid state MOS-FET devices for low leakage switching.

During one half-cycle of the demodulating waveform, one side of the input capacitor is grounded and e_{in} is stored on the capacitor. During the next half-cycle, the voltage stored on the input capacitor is transferred to the shunt capacitor, as a D.C. level which is proportional to the peak to peak amplitude of the in-phase square wave on e_{in} .

Filter

The output of the demodulator is fed to a 320 Hz filter. The filter attenuates both noise due to the detector and preamplifier and switching transients due to demodulation, and signal-to-noise ratio is thus improved.

The pulse rate used to drive the stepper motor is 400 pps.

FOLDOUT FRAME 1

DETECTOR VIDEO CHANNEL

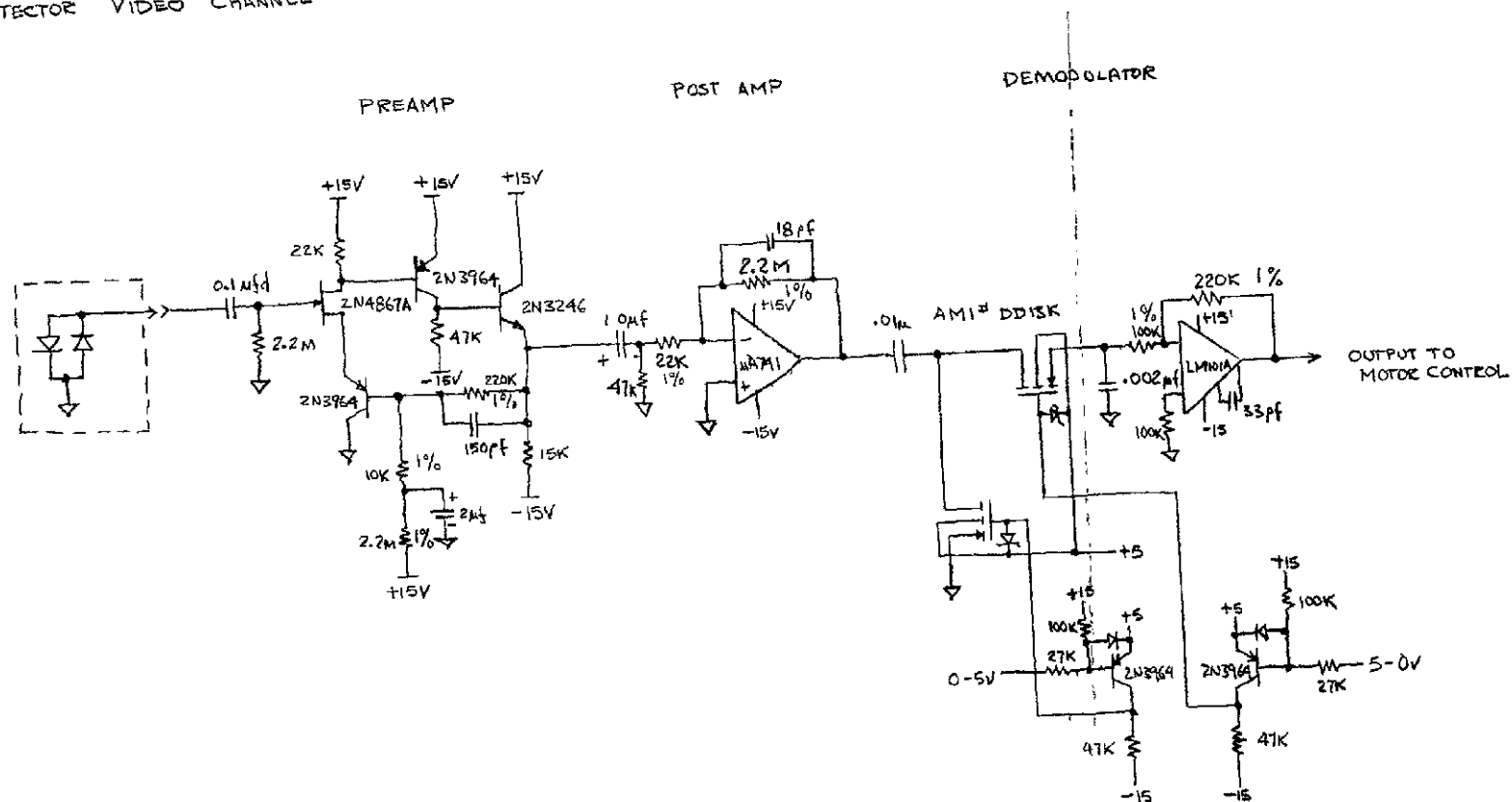


FIGURE 6-7 Video Channel Schematic

Threshold Detector

A circuit diagram of the motor control circuits is shown in Figure 6-8. After filtering, the signal is coupled to a positive and negative threshold circuit. The circuit will use an operational amplifier as a comparator with positive feedback to ensure a fast transition at the output. When the amplitude of the input signal exceeds the threshold level, the output of the comparator will change state. The discrete level change will be used as a gating waveform for motor triggers.

Gating Logic

The gating logic requires the coincidence of three signals to produce an output pulse. One signal is a positive output from the threshold circuit. The second signal is a positive level on the DISABLE bus. The third signal is a 409 Hz square wave. When the threshold level is exceeded and the servo is not disabled, the gating logic provides 409 Hz square waves to the appropriate motor stepping control. When the servo is disabled, a zero level on the STEP UP1 or STEP DN1 inputs causes the motor stepping control to step once in the indicated direction. INPUT requirements at the STEP UP1 and STEP DN1 are

| | |
|--------------------------|------------------|
| Zero level | 0.0v to + 0.5v |
| One Level | + 3.0v to + 5.0v |
| Duration at either level | 1.2 ms min |
| Rise time and fall time | 100 ms |

In the SLEW UP and SLEW DOWN modes of operation, appropriate gating external to the ATS connects the 409 Hz square wave from the counting circuits to the STEP UP or STEP DN1 inputs. The stepper motor will continue to step in the indicated direction at its slew rate of 1 step every 2.5 ms as long as the 409 Hz square wave is present at the STEP input.

Stepper Drive

The output pulses from the gating logic are applied to the stepper motor driver (Figure 6-9). The function of this circuit is to supply driving signals to the windings for the stepper motor in proper phase sequence in order to achieve error signal null.

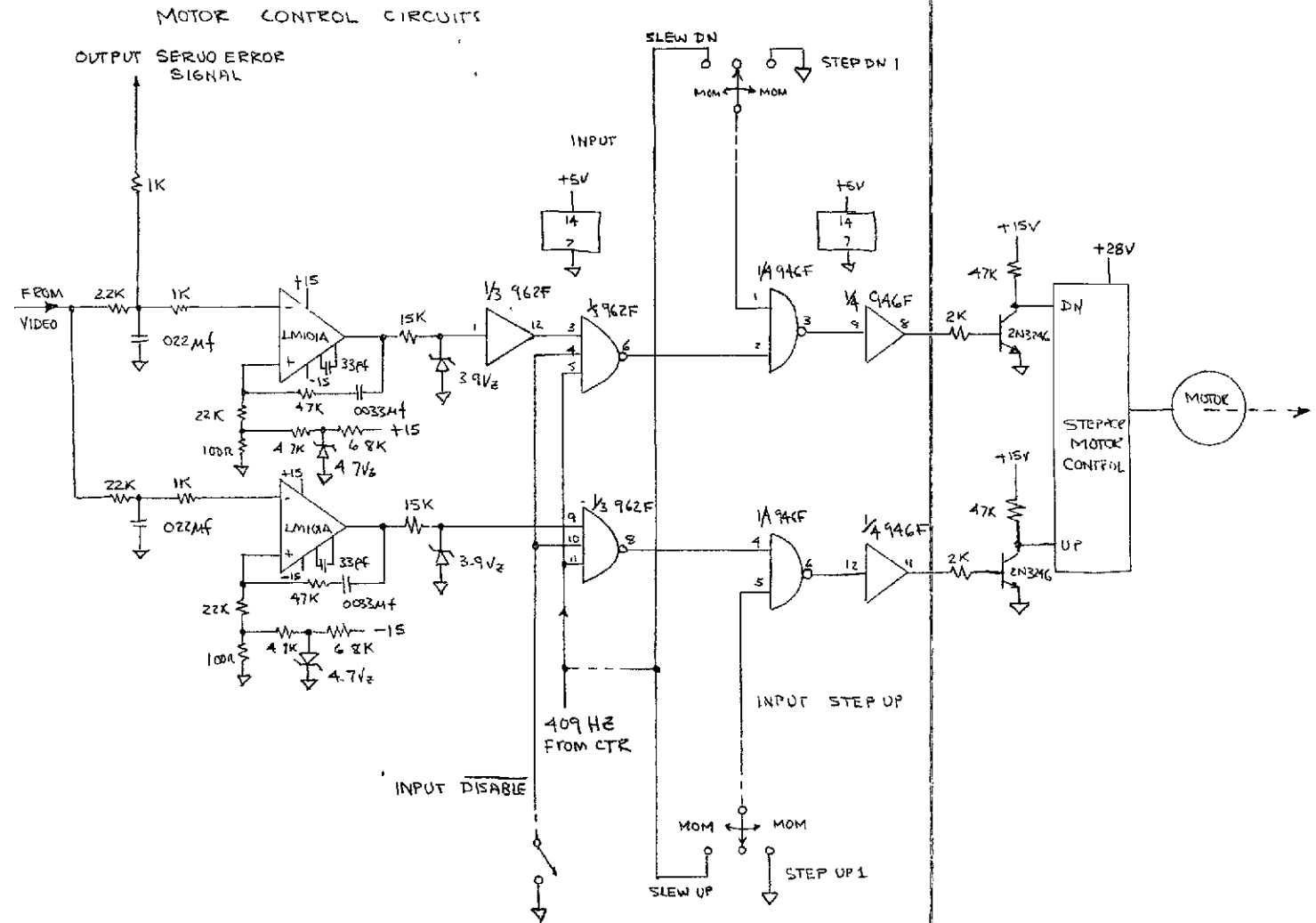


FIGURE 6-8 Motor Control Circuits

This page intentionally left blank

FOLDOUT FRAME 1

MOTOR STEPPER CONTROL

PRECEDING PAGE BLANK NOT FILMED

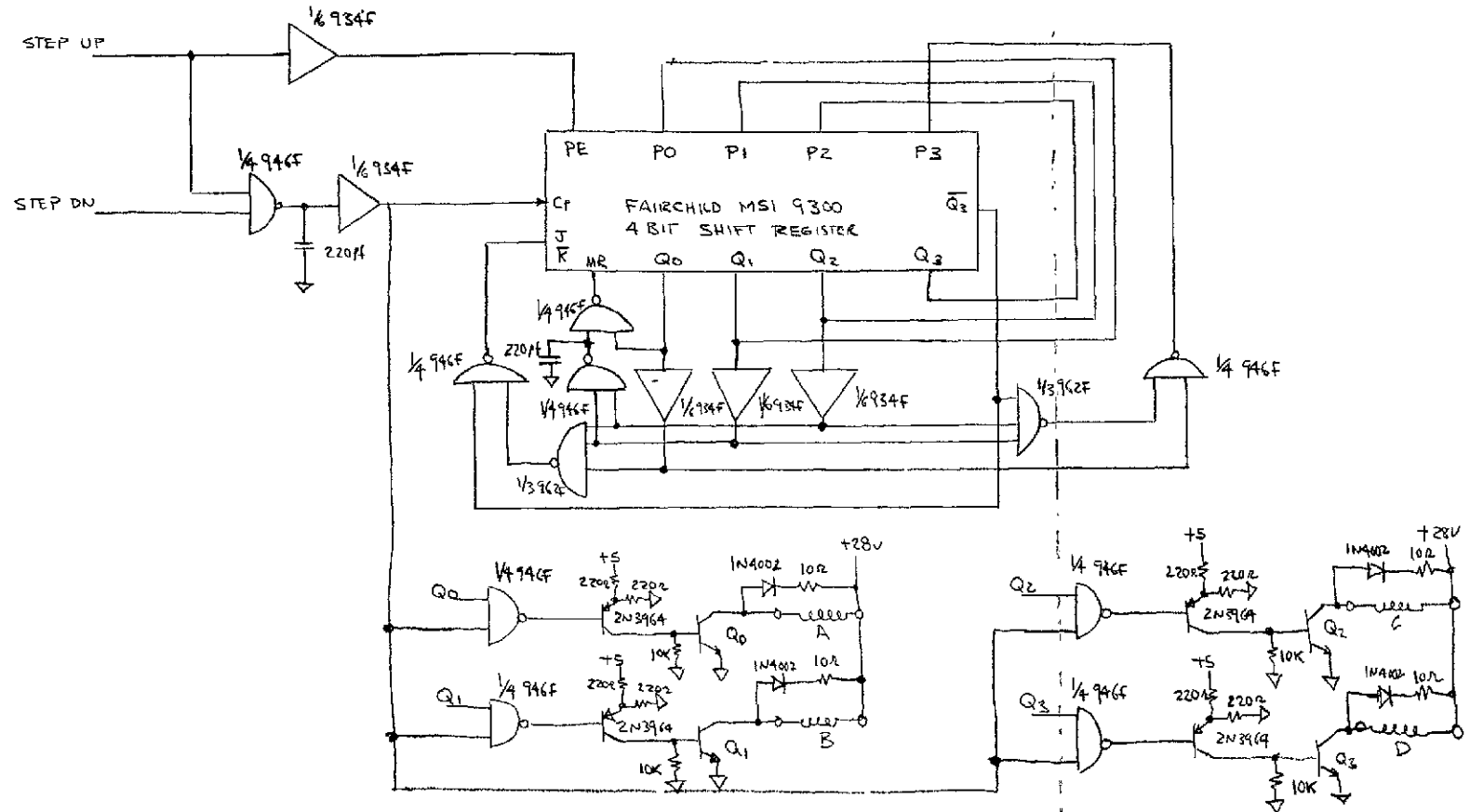


FIGURE 6-9 Stepper Motor Control

Resolver

The resolver driver is a buffer between the oscillator and resolver, presenting a high input impedance and low output impedance. Figure 6-10 shows the schematic. The multispeed sine-cosine resolver outputs are converted to a digital output using an approach identical to that used for the Antenna Electronics resolver encoding function, section 10.5.

Frequency Dividers and Light Drivers

Figure 6-11 shows the schematic for the dividers and the light source drivers. The carrier and demodulation frequencies of 1638 Hz and 819 Hz are derived from the input 16384 Hz pulse train. The input 16384 Hz square wave is counted down in a divide-by-ten counter circuit. The output of the counter circuit is taken as the expression $(Q_1 - Q_2) + Q_3$, which is equivalent to the decimal numbers 3 + 4, 5, 6, 7. This output is a square wave whose period is 1/10th the input square wave or 1638 Hz. This 1638 Hz is run through 2 divide-by-two counters to produce 819 Hz and 409 Hz for the second mod/demod channel and stepper motor control frequencies, respectively.

The square wave output of the frequency divider is applied to a current source for the GaAs emitter. Input voltage amplitude is regulated to maintain constant drive level for the emitter. The current source uses an operational amplifier with a transistor booster output to provide current to the diode.

Z-Axis Resolver Follower

To maintain accuracy in the X-axis channel, it is necessary that a pair of counter-rotating wedges slaved to the Z-axis remove Z-axis deviation from the X-axis light path.

To do this, a pair of wedges, resolver, stepping motor and motor control identical to the Z-axis set are placed in the X-axis light path. However, instead of deriving a signal from the Z-axis detector, the additional Z wedges are servoed to the output of the Z-axis resolver. Figure 6-12 shows the schematic.

The output of the Z-axis resolver, $E \sin \theta_z \sin 6440T$ is summed with the output of the Z-axis slave resolver, $-E \sin \theta_z \sin 6440T$. The summation is detected synchronously with the reference voltage, and the D.C. output of the demodulator is applied to threshold circuits identical to the Z-axis threshold circuits to control the gating logic to the motor step controller.

RESOLVER CIRCUITS

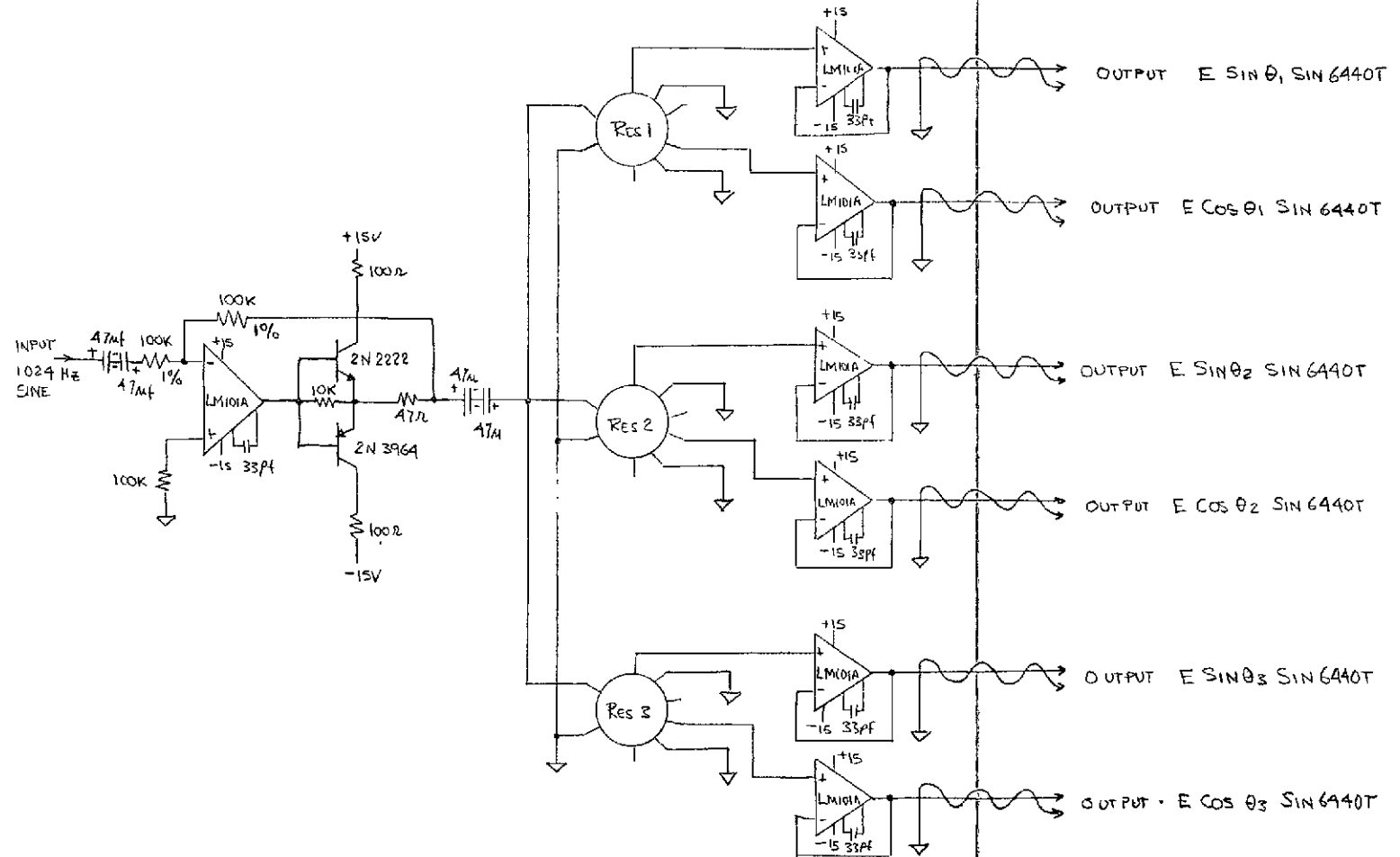


FIGURE 6-10 ATA Resolver Circuits

This page intentionally left blank

COUNTER CIRCUITS - LIGHT SOURCE DRIVERS

PRECEDING PAGE BLANK NOT FILMED

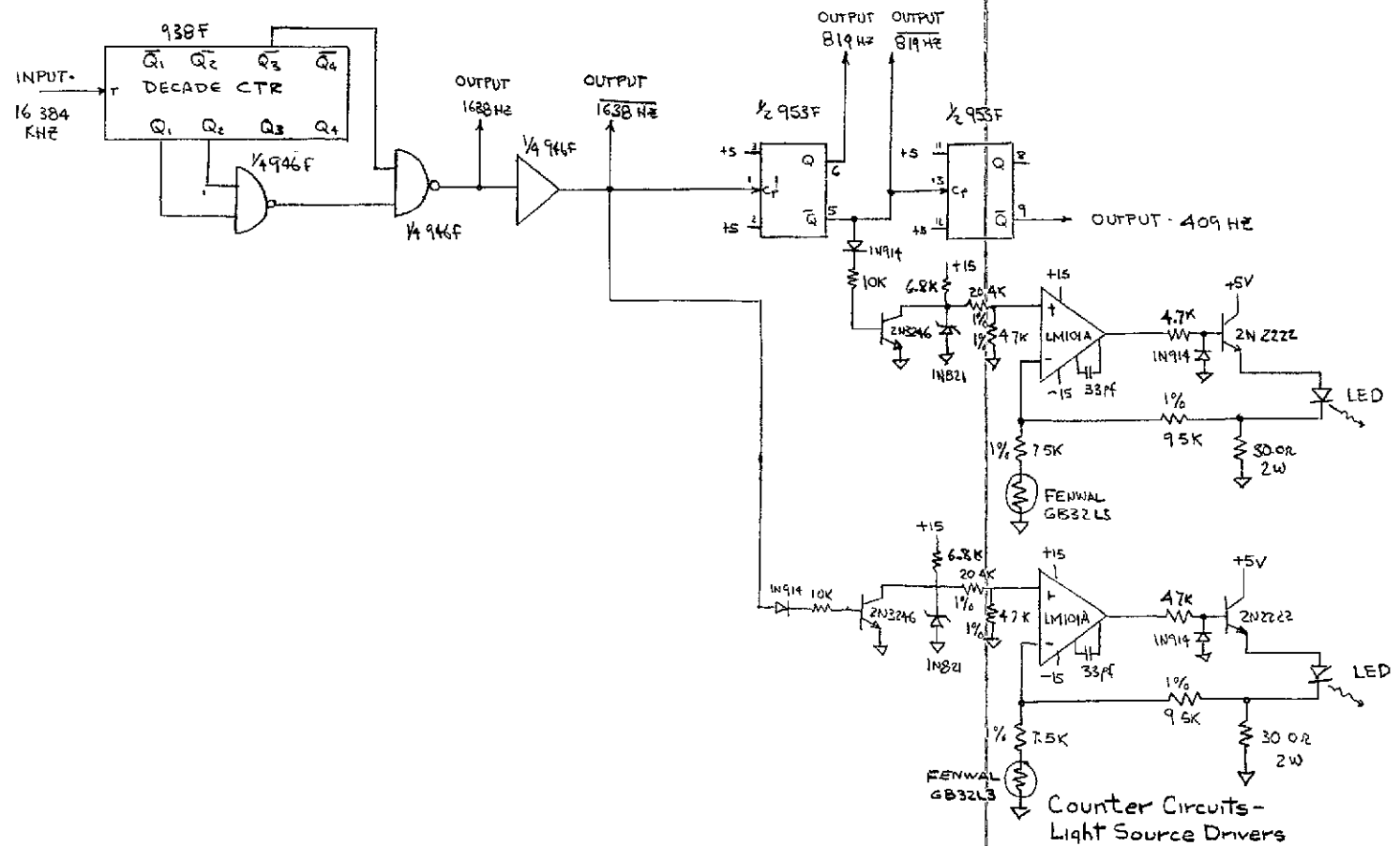


FIGURE 6-11 ATA Frequency Dividers and Light Source Drivers

This page intentionally left blank

Z AXIS RESOLVER FOLLOWER

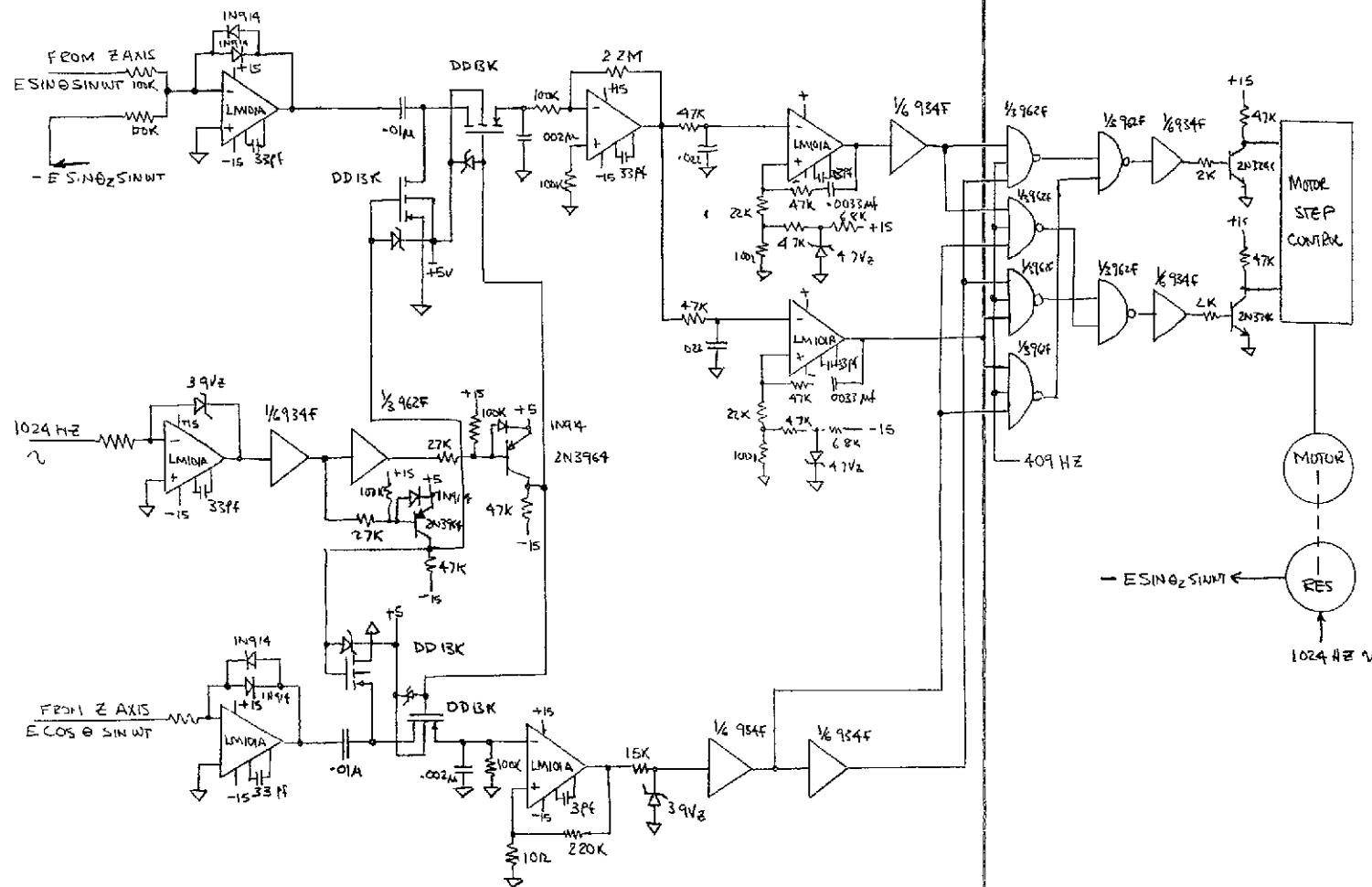


FIGURE 6-12 Resolver Follower

In the gating logic, it is necessary to switch the outputs of the threshold circuits so that either threshold can cause the motor to step up or down depending on the phase of the Cosine θ_z output of the Z-axis resolver, because in the 1st and 4th quadrants, if the slave resolver is ccw of the desired position, the summation voltage will be in phase with the reference. In the 2nd and 3rd quadrants the opposite is true.

The Cosine θ_z voltage output of the Z-axis resolver is in phase with the reference in the 1st and 4th quadrants and out of phase in the 2nd and 3rd. The phase of the Cosine θ_z voltage is detected by a demodulator synchronous with the reference. The output of the detector is positive or negative, depending on phase. This output is applied to a 0 volt threshold circuit, the outputs of which control the gating logic so that the servo drives in the correct direction to reduce the error in all four quadrants.

7.0 Digital Computer Assembly

7.1 Function

The Digital Computer Assembly (DCA) provides the computational, data storage, and data transfer capability for the PPCS. It provides the system monitoring and test capability. It also performs the telemetry and command processing for the PPCS.

7.2 Configuration

A modular redundant organization is utilized for the DCA as shown in the overall block diagram Figure 7-1. This concept achieves maximum lifetime and mission flexibility at minimum power and weight cost. A dual redundant data bus is used for all PPCS assemblies, except the Experiment Electronic Assemblies (EEA). Each bus has a separate terminal for each major assembly. The EEA's are served by dedicated data bus lines. Control of the data bus is through an Input/Output Processor (IOP). This unit also services the input/output requirements for telemetry and command. Control of the IOP is via the main memory which stores data bus, telemetry, and command control routines as well as data. Modularity is achieved through the use of a redundant parallel memory bus. This consists of 24 data lines plus 4 control lines which interconnect all of the DCA units. Memories are 8K x 24-bit plated wire units with

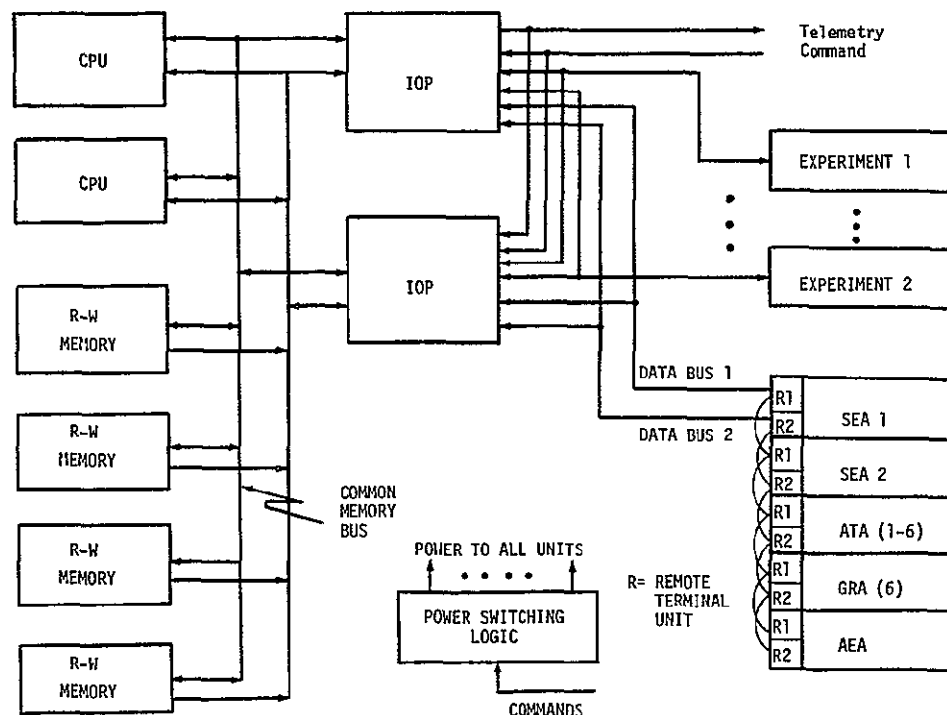


Figure 7-1 DCA/DATA BUS Redundancy Scheme

internal parity checking. All data transfer to and from memory is via the memory bus and conflicts are resolved at the memory. A MOS/LSI implementation is used for the CPU which is a 2's complement 24-bit machine. The CPU performs all of the application programs central to the PPCS operation and the data processing programs relating to DCA/DCA BUS operation as well. At any time, only one CPU, one memory bus, one memory module, and one IOP and one of the data buses is in operation. Selection of operating units is achieved by power switching of units. Any combination of the above units is possible.

7.3 Operational Description

As with other PPCS systems, the DCA is quiescent during launch and is activated upon PPCS turn-on. A restart interrupt is transmitted via the command link. This interrupt resets the CPU registers and begins processing at a fixed memory location. This location contains the software initialization module which bootstraps the PPCS system into full operation. A typical executive structure is shown in Figure 7-2.

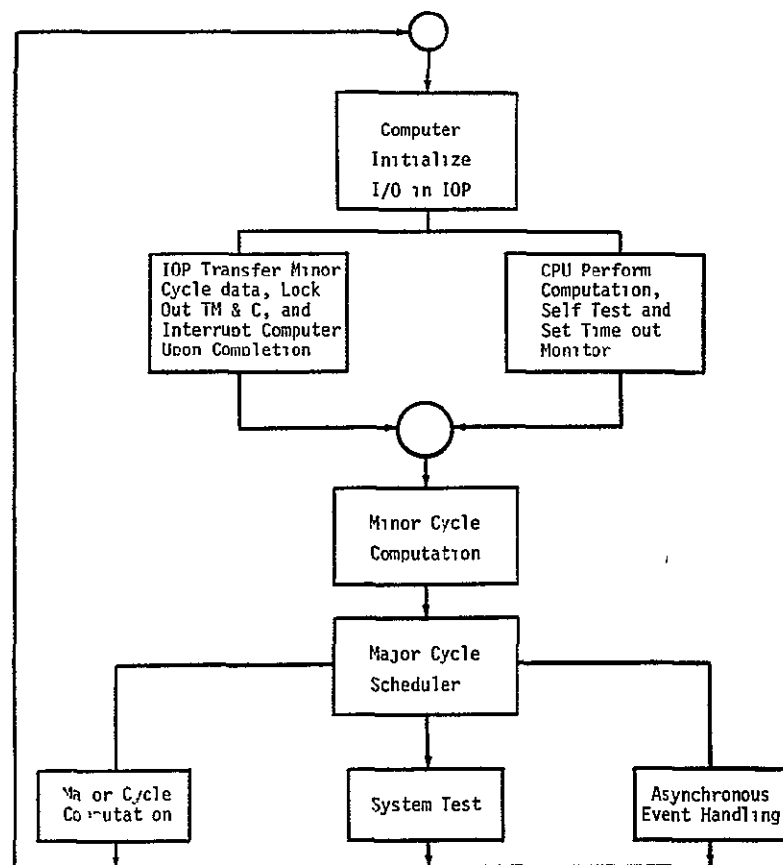


FIGURE 7-2 Typical DCA Executive Organization

Software Operation

At the beginning of a minor cycle, a real time clock interrupt causes the CPU to initialize the minor cycle. The CPU starts the minor cycle by requesting the IOP to provide the input data for the minor cycle. The CPU sets a time-out timer to monitor the I/O transfer. When the I/O is complete, the IOP interrupts the CPU to indicate the completion of data transfer. The CPU initializes the minor cycle as soon as the timer interrupt occurs. Under normal conditions, the self-test and the I/O data transfer should always complete before the timer interrupt. Therefore, the CPU always starts the minor cycle computation a fixed time after the start of the minor cycle.

Failure Detection

A number of failure detection modes for the DCA have been included. These include the CPU self-test timer, memory parity, power transient monitors and data bus error detection. The basic philosophy of the fault detection scheme is to quickly bring ground attention to bear upon a fault (or possible fault) and to aid in its diagnosis. A basic tool is thus the telemetry format and the information contained therein. Some of the diagnostic tools used for the DCA/DCA BUS are

| | |
|--------|--|
| Memory | Zero sum checks performed on program and other constant storage areas during self-test periods. Intermediate computations periodically transmitted via telemetry grouped so as to allow reasonableness checks. |
| CPU | Self-test performed on minor cycle and major cycle basis. All instructions and registers exercised with diagnostic results stored and telemetered. Zero sum checks and other memory checks also monitor CPU. |
| IOA | The data bus is checked by periodically sending data values to be D/A converted, then A/D converted in each Remote Terminal Unit and finally sent back to the CPU for checking. This is a partial check on IOP operation. Commands may also be sent from the ground which are turned and telemetered for comparison. |

IOP Operation

Computer Controlled Mode

This is the normal mode of operation where all IOP processing is performed under control of the CPU via the memory. There are 3 basic areas of memory

- 1) Data bus control - this memory segment contains the "idle" location and certain other small programs needed to fetch data. One such program is the minor cycle data gathering which is a fixed cycle of data bus addresses and the associated locations for storage.
- 2) Telemetry control - the PPCS telemetry format is stored in this area in a sequence of IOP instructions. Locations are provided for all current data. The CPU, in its normal processing, keeps these locations refreshed with the latest values.
- 3) Command control - this sequence of memory locations contains the sequential commands as received. In some cases, the CPU simply places these into the data bus area, while others may result in a number of data bus commands. These are normally serviced only during the major cycle operation.

Memory Reload

To accomplish loading of memory locations for targeting, alteration of star tables, and entering of other constants, use is made of the command channel. This data is stored in the command control area. The normal command servicing routine of the CPU recognizes this data as memory load. Checks may then be performed for data validity and the data shuffled to the commanded locations by the CPU. This approach to memory reload simplifies the IOP implementation and memory protection problem.

Backup Mode

Certain discrete commands are distinguished by the IOP deviating it from the normal mode. One of these engages the ROM which provides a backup program. In this mode a fixed data bus format is carried out and the resulting data placed on telemetry. Commands are acted upon immediately and transmitted on the data bus. Thus the main memory and CPU are bypassed entirely while the IOP is in this mode.

7 4 Performance Characteristics

The Digital Computer Assembly performance characteristics, based on the projected 1975 technology, are summarized in Table 7-1

TABLE 7-1 DCA Performance Characteristics

| | | | | |
|-------------------------------|---------------------------------------|-------------------|------------------|------------------|
| DCA type | General purpose, digital computer | | | |
| Arithmetic | 2's complement, fractional arithmetic | | | |
| Addressability | Directly to 32 K | | | |
| Data word | 23 bits plus sign | | | |
| Instruction word | 24 bits, single address | | | |
| Number of Index registers | 3 | | | |
| Typical Instruction Times | | | | |
| Add without indexing | 3 μ sec | | | |
| Add with indexing | 4.5 μ sec | | | |
| Multiply | 24 μ sec | | | |
| Divide | 40 μ sec | | | |
| Memory type | Magnetic wire | | | |
| Cycle time | 1.5 μ sec | | | |
| Memory word length | 24 bits | | | |
| Memory capacity | 8096 words/module | | | |
| Access time | 1.5 μ sec | | | |
| Read access time | 0.5 μ sec | | | |
| Physical Parameters | | | | |
| | Reliability (Three year) | Power* (watts) | Weight* (lbs) | Size* (cu in) |
| CPU (two, one on) | .9840 | 10 | 10 | 240 |
| IOP (DIA) (two, one on) | .9826 | 10 | 8 | 180 |
| Memory (8K) (four, one on) | .9973 | 13 | 18 | 480 |
| Memory Bus (two, one on) | .9986 | 5 | 4 | 120 |
| DCA including redundancy | .9629 | 38 | 40 | 1020 |

* Power supplied

7 5 Design

This section describes the design of the DCA and IOP

7 5 1 Instruction Format

a. Class I Instructions



wherein

f function code (5 bits)

x Index field, expandable from 1 bit to 3 bits A typical 2-bit x field is decoded as follows

x = 00 no indexing

01 indexed by X_1 , $Y = (X_1) + y$

10 indexed by X_2 , $Y = (X_2) + y$

11 indexed by X_3 , $Y = (X_3) + y$

y address or direct operand field, expandable from 12 bits (for a word length of 18 bits and an x field of 1 bit) to 17 bits (for a word length of 24 bits and an x field of 2 bits)

Y effective operand address

X_i i^{th} index register, $i = 1, 2, \text{ or } 3$. The register length depends on the maximum memory capacity

b. Class II Instructions



wherein

f equals 11111

g subfunction code (5 bits)

n a constant field to specify shift count, justification limit, skip conditions, or immediate operand

7.5.2 List of Instructions

The list of instructions is summarized in Tables 7-2 and 7-3

TABLE 7-2. List of Class I Instructions

Add (ADA)
 Subtract (SUA)
 Multiply
 Divide
 Multiply and Round
 Add Double Precision (ADD)
 Subtract Double Precision (SUD)
 Add to Memory
 Load (LDA)
 Load Double Precision (LDD)
 Store (STA)
 Store Double Precision (STD)
 And (Logic Product) (AND)
 Inclusive or (Logic Sum) (IOR)
 Add to Index Register with Skip
 Load Incremental Timer or Index Register (LDX)
 Store Index Register or Zero (STX)
 Tally Memory with Skip
 Store Status Register (STS)
 Load Status Register (LDS)
 Jump on Accumulator Overflow
 Jump on Zero
 Jump on Positive
 Jump on Negative
 Jump on Zero Double Precision
 Subroutine Jump
 Indirect Subroutine Jump
 Indirect Return Jump
 Unconditional Jump or Index Jump
 Compare
 Compare Double Precision

TABLE 7-3. List of Class II Instructions

Add Immediate
 Load Accumulator Immediate
 Load Index Register X_1 Immediate
 Load Index Register X_2 Immediate
 Load Index Register X_3 Immediate
 Two's Complement
 Two's Complement Double Precision
 Absolute
 Absolute Double Precision
 Left Shift Zero-field
 Right Shift Zero-field
 Left Shift Circular
 Left Shift Zero Filled Double Precision
 Right Shift Zero Filled Double Precision
 Left Justify
 Left Justify Double Precision
 Skip
 Halt
 Input with Skip
 Output with Skip

7 5 3 Central Processor Unit

Organization and Block Diagram

The organization of the central processing unit is modular and bus oriented. It is partitioned for LSI implementation. The CPU block diagram is shown in Figure 7-3.

Since the MOS/LSI circuit speeds are slow and maximum performance is required of the processor, the normal computer arithmetic unit is replaced by two arithmetic units. Each unit is preassigned a specific task in executing an instruction and both work in parallel.

The "Operand Arithmetic Unit" (OAU) performs arithmetic and data handling associated with computer data. The Program Arithmetic Unit (PAU) performs similar functions on program addresses and program control words.

The controlling of these two units in conjunction with the memory system and Input/Output is the responsibility of the control modules or chips. These control modules shall decode all of the instructions and generate the control signals necessary for the operation of the processor. The control modules are somewhat flexible in that the instruction repertoire can be broken up in many ways so as to meet pin and chip size restraints.

The OAU, besides containing an accumulator and multiplier - quotient register, also requires a holding register (D reg) and a second multiplier register. The latter register is necessary in order to execute multiplication in the specified time.

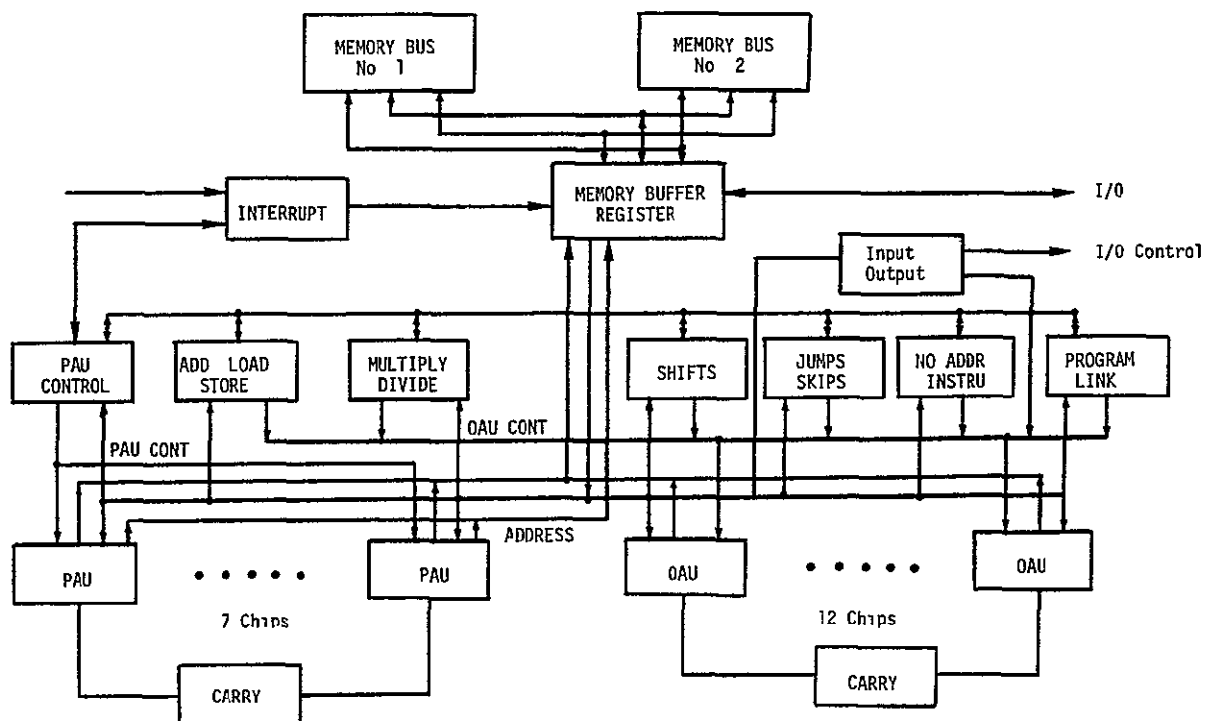


FIGURE 7-3 CPU Block Diagram

Overlapped Instruction

An instruction fetch-execution overlapping scheme is employed such that while the PAU is modifying the address of the next instruction, the OAU is executing the present instruction

Logic Partitioning

The partitioning of the CPU into modules or LSI chips is directed towards minimizing both the number and number of types of modules or chips. For example, the same carry module is used in both the Operand Arithmetic Unit (OAU) and in the Program Arithmetic Unit (PAU). The OAU itself is made up of two bit arithmetic unit slices, as is the PAU. The method of partition is quite flexible. The computer's word length can be modified by changing the number of OAU modules, up to a maximum of 30-bit words. The address field may increase by adding PAU chips up to a maximum of a 16-bit address, which would directly address 65,000 words. The number of index registers may be increased in 4 register increments by adding a set of PAU modules.

Add Type Control Module

This module is used to control the memory, Program Arithmetic Unit (PAU), and Operand Arithmetic Unit (OAU) for simple instructions such as STA, STD, STS, STX, LDA, LDD, LDS, LDX, ADA, SUA, ADD, SUD, AND, IOR. A block diagram of the control module is shown in Figure 7-4. The module implements seven register elements which hold the five instruction op-code bits and the two index register bits during the execution of an instruction. The instruction is decoded and an operand memory cycle is initiated by this module if it is one of the instructions listed above. If it is not one of the instructions listed above this control module does nothing. If the operand address of the instruction is to be modified by the contents of the index register, the initiation of the operand fetch memory cycle is delayed by one clock period, unless the instruction is STA, STD, STS, or STX.

The initiation of the memory cycle to fetch the next instruction is controlled by this chip if the previous instruction was one of those listed above. Also, all the control functions required by the Operand Arithmetic Unit for the execution of the above listed instructions are generated on this chip.

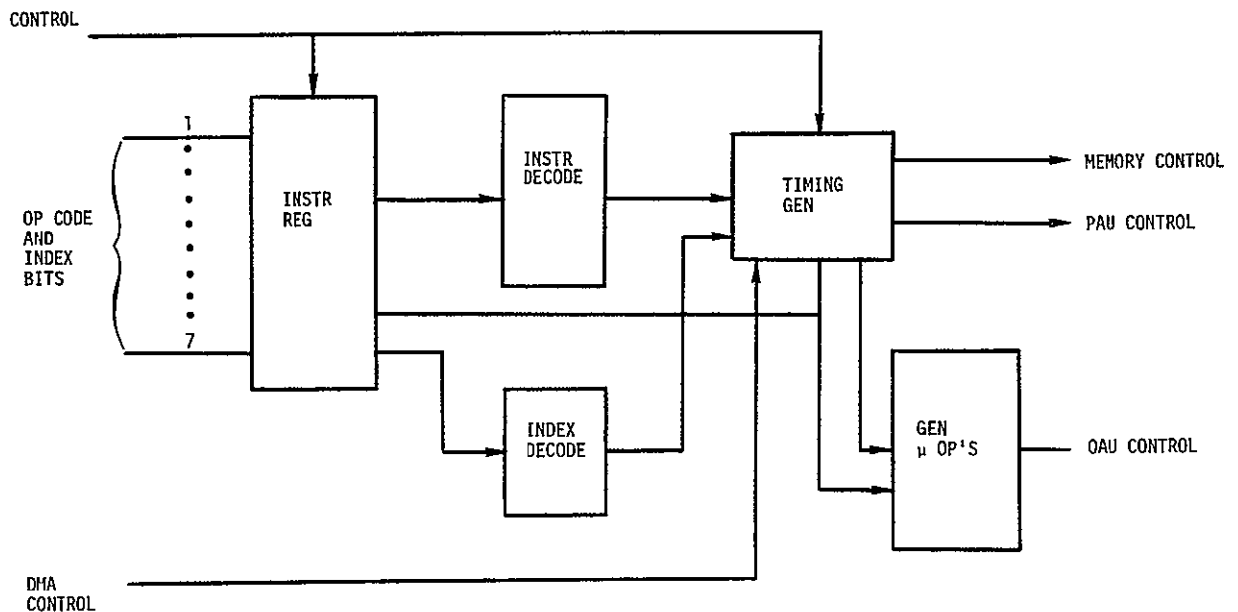


FIGURE 7-4 Control Module for Simple Instructions

Carry Module

Since the PAU and OAU are partitioned in such a way as to have two bit "slices" of arithmetic on each module or LSI chip, the carry module is used to simultaneously generate carries for up to 16 OAU modules. This allows an arithmetic unit to be made for up to 30-bit operands. Each OAU chip supplies a carry pass and a carry generated signal to the carry chip, and receives from the carry module a carry signal. Two identical modules are required for the carry function. Each of these modules accepts 17 carry generate, and 16 carry pass signals, and generates 8 carry outputs. This carry module will also be used in the PAU, when indexing (adding the contents of an index register to the address field of an instruction) and arithmetic with index registers are performed.

Program Arithmetic Modules

The PAU modules perform the following operations

- 1) Computing the effective address of an instruction, i.e., adding the contents of a specified index register to the address of the instruction, when required.

- 2) Incrementing the program counter. This operation occurs while each instruction is being fetched, and when a skip occurs (e.g., ADX, SKP, CAS)
- 3) Adding to the contents of an index register (e.g., ADX)
- 4) Output the contents of the program counter, or an index register (e.g., STX)
- 5) Load the program counter, or an index register, from the address field of an instruction (e.g., JMP, JAZ, LXI)
- 6) Loading an index register or program counter, from a memory location (e.g., LDX)
- 7) Temporary storage of address information (e.g., JMP, JAZ, LXI, and in case of Direct Memory Access between instruction fetch and instruction execution).
- 8) Decrement index register (e.g., JMP)

Each PAU module thus contains two bits of each of five registers, an adder, and logic trees to supply inputs to the adder, data bus, address bus, and registers. A minimum of control logic is included on this module (e.g., index register select control) in order to increase speed. A block diagram of the Program Arithmetic Unit module is shown in Figure 7-5

Operand Arithmetic Module

The operand arithmetic module consists of two bits of the A register, 0 register, adder and gating into the A, Q, and adder. Twelve chips are required for a 24-bit computer.

Normally 3 data registers are required to perform MPY and DVD. The OAU chip is being designed so that only two data registers are required. The inherent delay in the adder is used as storage for the partial product or remainder when performing MPY or DVD respectively. The block diagram is shown in Figure 7-6

Other Modules

Table 7-4 lists the module types required for the conceptual CPU design and the estimated number of modules. It should be noted that those modules whose characteristics are critical, such as OAU, PAU, and carry modules, have been conceptually designed.

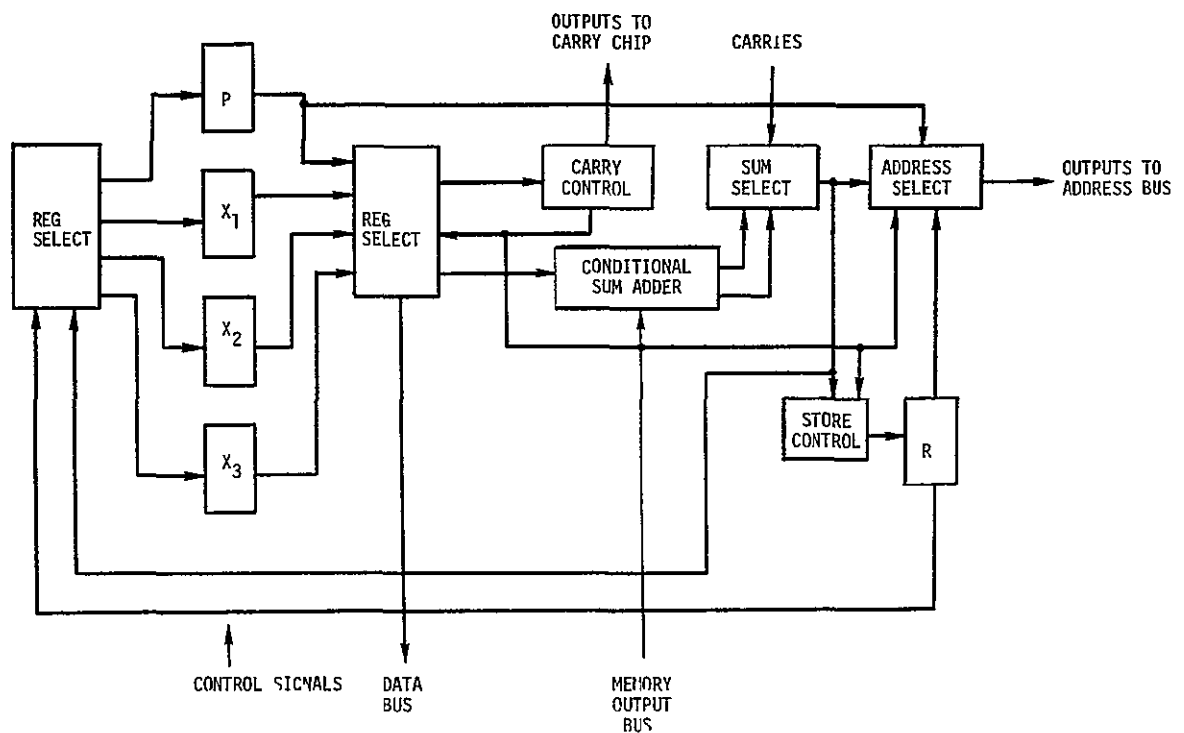


FIGURE 7-5 PAU Module Block Diagram

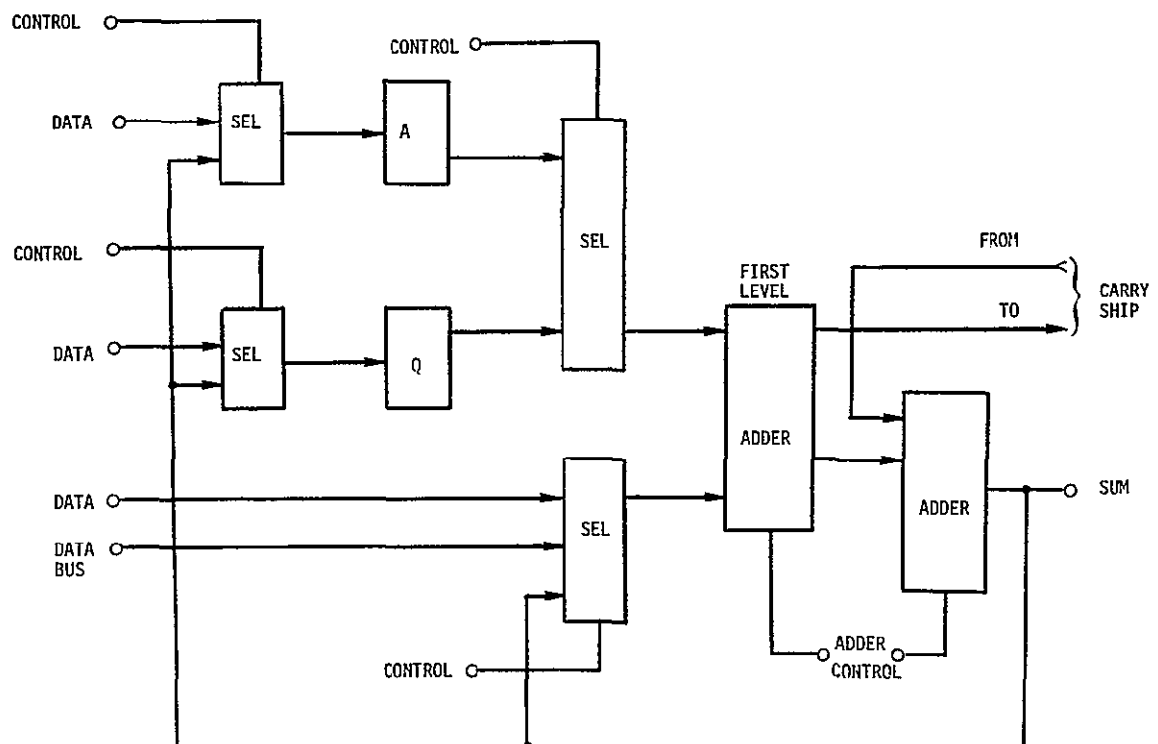


FIGURE 7-6 OPERAND Arithmetic Module

TABLE 7-4 CPU LSI Modules

| Module Type | No Required |
|-------------------------|-------------|
| Operand Arithmetic Unit | 12 |
| Program Arithmetic Unit | 7 |
| Carry | 4 |
| PAU control | 2 |
| Add control | 1 |
| Multiply control | 1 |
| Shift control | 1 |
| Jump control | 2 |
| Program link | 2 |
| No address control | 1 |
| I/O | 2 |
| Interrupt | 1 |
| Contingency | 4 |
| Total | 40 |

7 5 4 Memory System Design

A memory with a basic capability of 8,192 24-bit words of plated wire magnetic storage is considered here. The plated wire element used as the storage device provides a non-destructive readout capability assuring a more reliable restore of information as compared to destructive readout memories. The memory system is inherently non-volatile and by design could be resistant to high levels of nuclear radiation. A cycle time of 1.5 μ sec, with a read access time of 500 nsec is expected.

General Memory Organization

The plated wire memory is basically organized in a linear select word-oriented system. A multiple word readout is utilized which accesses multiple words under a word strap. Decode at the data bit sensing selects the desired words' contents, dropping the contents of those words not desired. The NDRO characteristics of the plated wire element allow this procedure to be used thereby reducing the word driver electronics compared to linear select schemes using DRO storage elements. Stacking of eight computer words under one word strap has been used in existing designs. The system organization is shown in the

following block diagram, Figure 7-7.

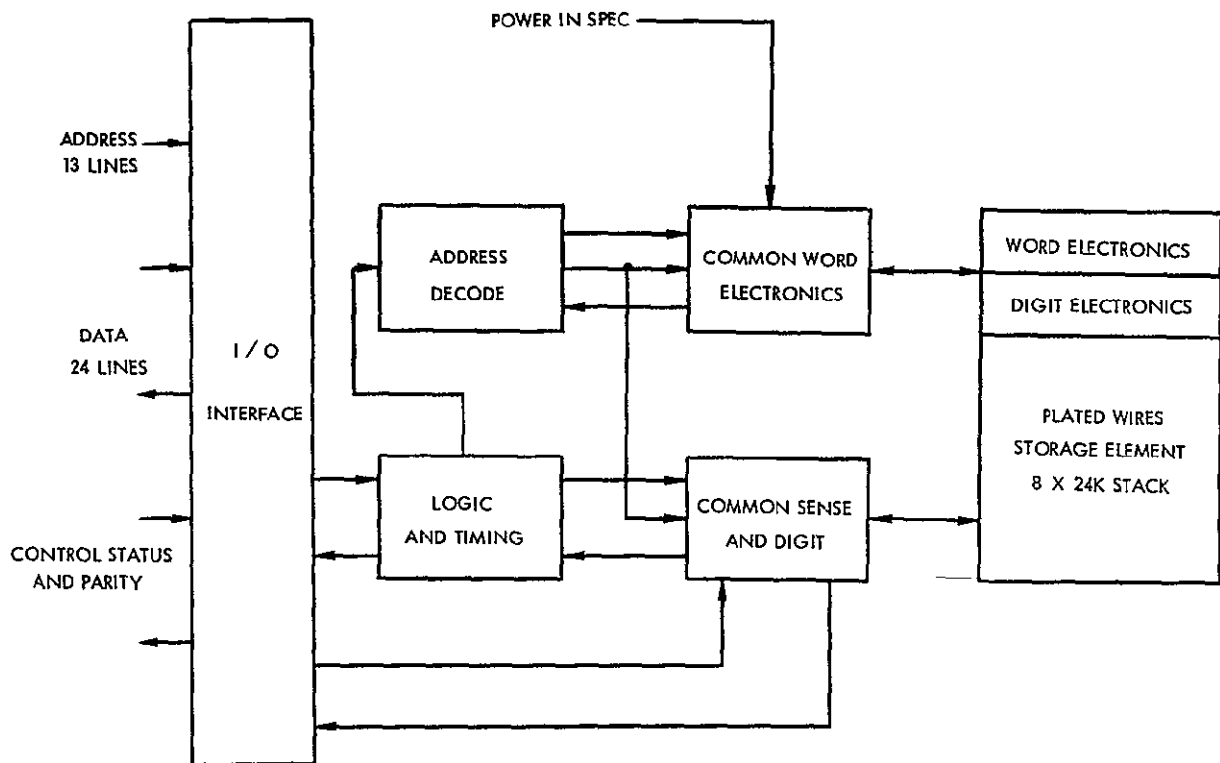


FIGURE 7-7 Memory System Block Diagram

7.5.5 DCA Memory Bus

The memory bus connects four R-W memory units, two central processing units (CPU's), and two Input/Output Processors (IOP's). In order to provide sufficient redundancy to approach the desired reliability, the computer modules are interconnected using a pair of DCA internal busses. Each internal bus consists of 24 data and four control lines, properly terminated to avoid reflections. These lines will be driven through diodes in order that the line drivers disconnect themselves when they are not in use. The line receivers should also be connected to the line through diodes, so that they

can be disconnected from the line by power switching. This bus system is illustrated in Figure 7-8. Bus delay will be of the order of 250 nsec

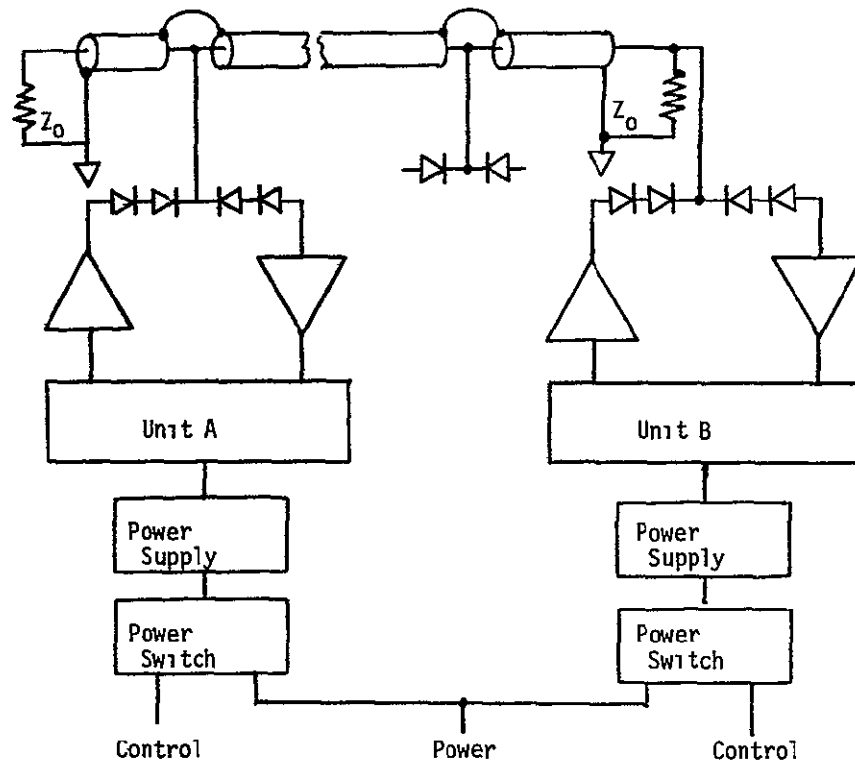


FIGURE 7-8. Memory Bus

7.5.6 Input/Output Processor

The Input/Output Processor (IOP) provides interface to the CPU via the memory bus as described above. Other interfaces are with the PPCS data bus and with telemetry and command. These are shown in the IOP block diagram, Figure 7-9.

Organization

The IOP is designed so as to be controlled directly from a program stored in memory. A dedicated memory area is used for input/output, containing a mixture of IOP instruction words and data. The CPU loads data into appropriate locations and may modify the IOP program when necessary due to failures or

system mode changes. A dedicated memory location must be continually monitored by the IOP when idle, awaiting control by the CPU

In addition, the IOP will be controllable by a Read-Only Memory (ROM) for use in failure modes. The ROM will contain an IOP instruction program to allow data bus operation, telemetry, and command operation

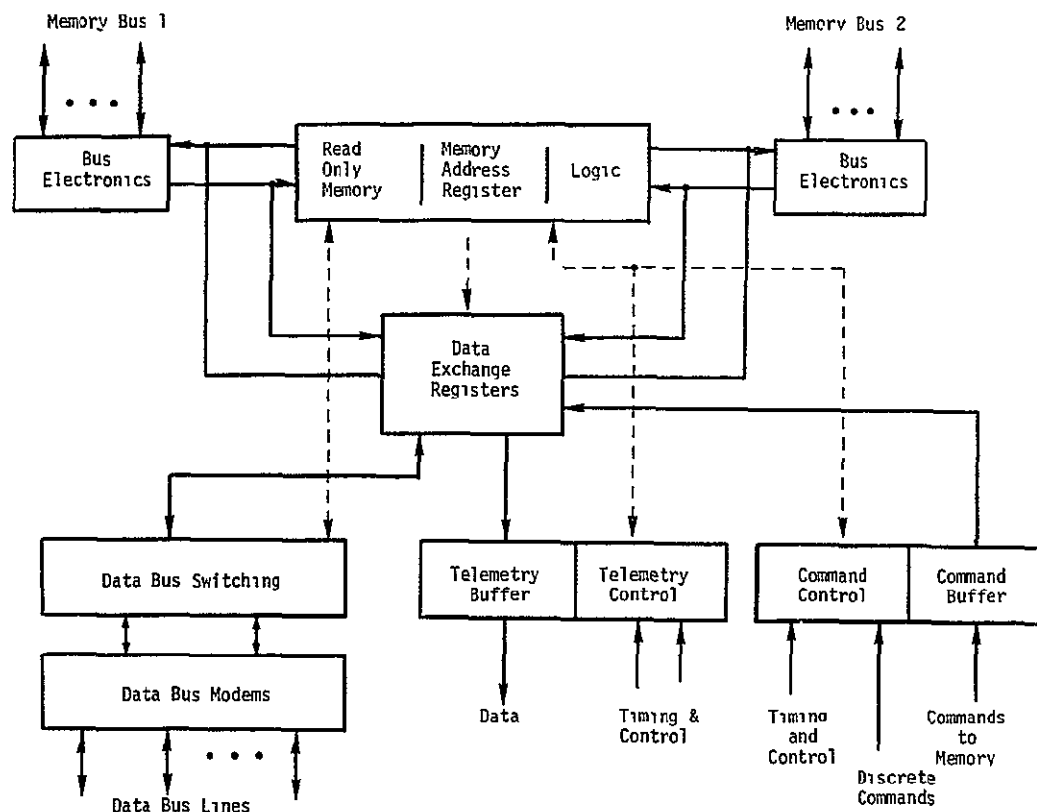


FIGURE 7-9 Input/Output Processor Block Diagram

Command Processing

It is assumed that commands will have the same format as data bus words, i.e., each command message will be in bytes with a parity bit on each byte and a longitudinal parity byte on the whole message. Each command will be checked for parity before execution. Most commands for PPCS will be destined for main memory where they will be acted upon by the CPU. The IOP must also accept some discrete commands which provide a PPCS command path external to the CPU. The PPCS command format will consist of an address consistent with

the data bus format. This simplifies the CPU processing required and provides some failure immunity. The command portion of the IOP must contain a register large enough to hold a command plus its address. These must be buffered to resolve conflicts on the memory bus and data exchange register. The control logic will provide priority for the commands within the IOP over data bus and telemetry. A buffer fullness indicator is not required to the IOP control due to this precedence.

The command control provides logic to gate the asynchronous command bits into and out of the command buffer. There is also an interrupt from the IOP to the CPU indicating the presence of new command data. This interrupt is set upon receipt of each longitudinal parity.

Telemetry Processing

The telemetry system operates asynchronously to the PPCS. Hence, the telemetry unit in the IOP must request more data when its buffer is nearing empty. Data is clocked out of the buffer by telemetry clock and in by the IOP clock. The necessary synchronization is performed by the telemetry control unit. A "buffer low" signal tells the IOP control to access new data from memory. In this way, the IOP can continually service telemetry without any CPU intervention at all.

Under normal operation, the telemetry unit has immediate precedence in the IOP above data bus and below commands. In the backup mode, the telemetry input comes directly from the data bus, through the data exchange register, under control of the ROM program.

Data Bus Processing

In the computer control mode of operation, the IOP will interrupt its data bus management to service command or telemetry requirements. At the end of all data bus traffic control returns to an "idle" location in main memory. When the CPU wants to send or receive data via the data bus, it stores an appropriate instruction in this location branching the IOP to the appropriate routine.

When data is transmitted on the data bus, switching is performed dependent on the address. IOP control switches to the appropriate EEA or to the PPCS data bus and its associated modem. The modem function includes parity generation and synchronization for the data bus.

For data coming into the computer from the data bus, the switching is still set up from the immediately preceding "REQUEST" message. Parity is checked in the modem. Upon detection of a parity error, the IOP shall store its program address in a dedicated main memory location and interrupt the CPU. After a specified pause, the IOP control continues with its operation taking its next instruction from a location specified in the dedicated memory location.

The memory location for storage must be maintained in the control unit, as specified by the previous instruction.

IOP Control

The control unit of the IOP monitors the status of the IOP and directs data accordingly through direct control of the data exchange register. Each memory request is initiated by the control unit and the response monitored to distinguish data from instructions. The latter words are decoded and the control unit logic set up to perform this action.

Memory address registers are provided in the control unit for command, telemetry, and data bus control. Incrementing of each is handled separately.

The ROM provides the entire IOP program in the backup mode when directed by discrete commands via the command control logic.

8 0 Data Bus

8 1 Function

The data bus provides data formatting and data transmittal for all data exchange between other PPCS assemblies and the digital computer. Analog to digital and digital to analog conversion, serial to parallel conversion, and line driving functions are included.

8 2 Configuration

A data bus configuration where all data exchange is over one or two twisted pair lines is used to minimize spacecraft wiring. A general configuration is shown in Figure 8-1.

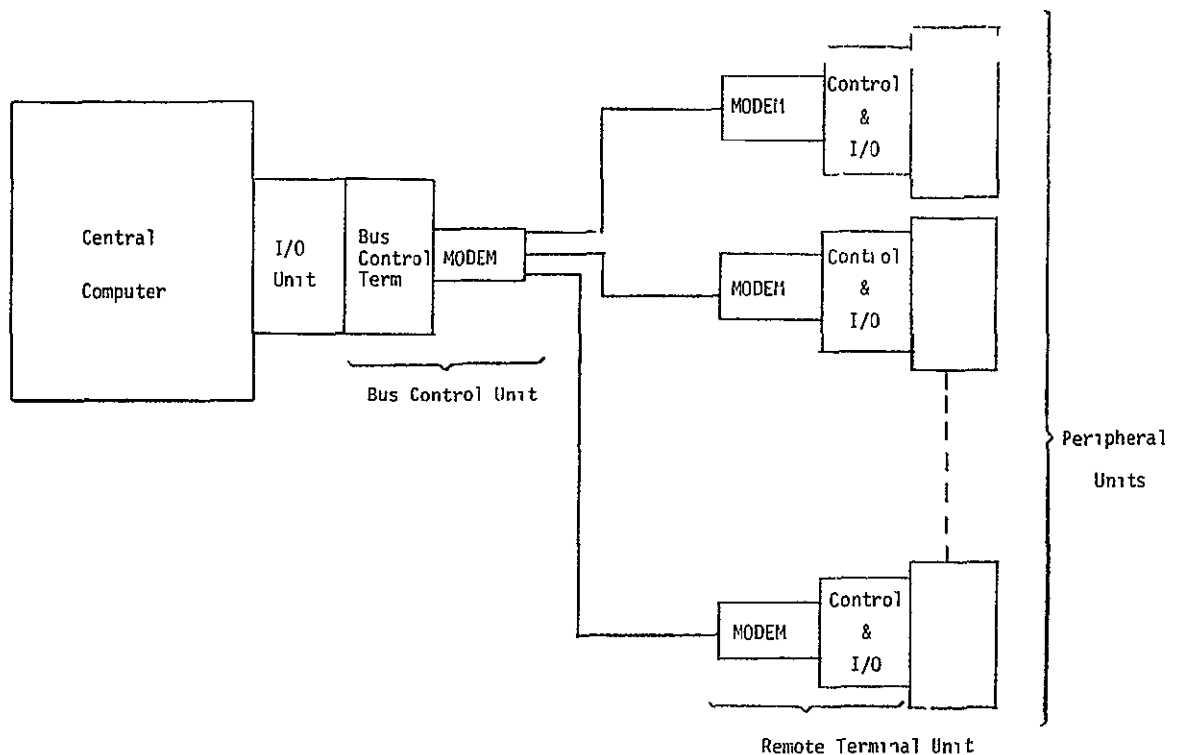


FIGURE 8-1 Generalized Data Bus

Master control of the bus is by the bus control terminal (BCU). Each peripheral unit to be communicated with has a remote terminal (RTU) as its communication portal. Communication occurs between the BCU and one RTU at a time by serial data transmission. One twisted-pair line is used for transmission in either direction. A second line carries a master clock from the BCU to all the RTU's. Transmission on the data line at 500 kilobits per second in biphase (Manchester-Ferranti) code permits the use of transformer coupling to the line from each of the modems. A modem serves the function of transmitting and receiving line data, and of encoding and decoding between biphase code and conventional binary as used within the RTU proper.

Primary control of the bus traffic is by the BCU. Data is transmitted to a given RTU as specified by an address at the beginning of transmission. Receipt of the completed message is signified when the RTU replies with its own address. For data from a RTU to the BCU the BCU first addresses the desired RTU and then requests the data. The RTU replies with its own address, and then the requested data. The system also features error detection in the form of horizontal and vertical parity checking.

A packaging configuration for the PPCS data bus remote terminals has not been developed. The terminals are primarily MSI/LSI packages (except for the line drivers/receivers) and could easily be packaged within a slice of each electronics assembly. Since each remote terminal will probably interface with more than one user, a small electronics package located near each user may be a desirable configuration.

8.3 Operational Description

The data bus is quiescent during spacecraft launch and initial orientation. Following PPCS turn-on, the data bus is active - all traffic is controlled by the computer. Two data bus operating modes are distinguishable. The normal mode uses messages with multiple bytes with the remote terminal programming the source/destination of the data through use of its read-only memory. If this ROM fails, an override mode is provided whereby the ROM is bypassed and data exchange is accomplished byte-by-byte with a computer request needed for each byte. Operation in this mode is considerably slower.

8 4 Performance Characteristics

Data bus performance characteristics are summarized in Table 8-1

TABLE 8-1 Data Bus Characteristics

| | |
|---|---|
| Bit Rate | 500 kHz |
| Word Size | 8 bits + parity |
| Format (on line) | Serial, semi-duplex (two way traffic, one way at a time) |
| Coding | Biphase |
| Transmission Line | Twisted, shielded pair, Transformer coupled |
| Number of Lines | 2 (clock and data) |
| Bus Efficiency | 50% (estimated) |
| PPCS Load (% of available capacity presently used) | 16% |
| Control Scheme | Central control by computer |
| Error Control | Vertical and Horizontal Parity |
| Terminal Capacity | |
| Computer to User | Any combination of 16 analog or digital (8 bit) words |
| User to Computer | Any combination of 32 analog or digital (8 bit) words |

8 5 Design

The remote terminal is organized into a modem section, a control section, and an input/output section (Figure 8-2)

Modem

The modem serves as the coupler and decoupler to the bus. The data bus signal is a biphase (Manchester-Ferranti) coded signal having a voltage swing of 5 to 10 volts peak-to-peak. When receiving, the modem decodes this to standard binary serial shift format. It also generates a two-phase clock from the clock bus line for use by the RTU's MOS/FET logic. Provision is also made to detect the beginning of a BCU message and reset of the RTU logic for interpretation of address and function code. When transmitting, it converts the RTU's data to biphase code, and drives the line at suitable impedance levels. Coupling to and from the line is via the same transformer.

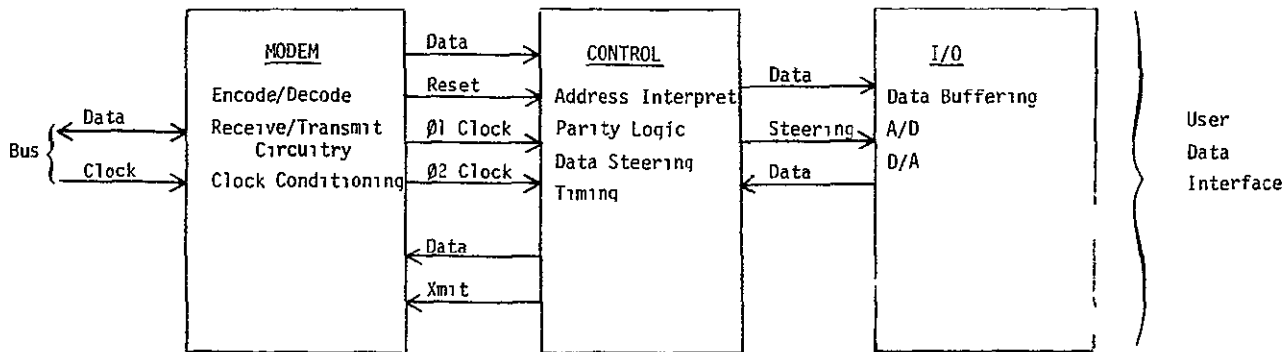


FIGURE 8-2 General Organization of the Remote Terminal Unit

Message Format

Standard message format is shown in general form in Figure 8-3. The message is divided into bytes, each byte consisting of 8 functional bits plus one horizontal parity bit. The message begins from the BCU with the address of the RTU being called. The second byte contains a function code (to be explained later). There follows zero to 16 bytes of data. The last byte of the BCU's transmission is a vertical parity over all prior bytes. The RTU's reply begins with its own address, followed by zero to 32 bytes of data. The message ends with a vertical parity byte.

Although two-way data is in general possible, it has seemed more convenient in PPCS at this time to limit traffic to one-way transactions, leaving more design freedom in the I/O control. In the case of BCU - RTU data, the RTU replies only with its address to signify valid receipt. In the case of RTU - BCU data, the message sequence is

| | |
|-----|-----------------|
| BCU | Address |
| | Function Code |
| | Vertical Parity |

RTU Address (its own)
 Data (0 - 32 bytes)
 Vertical Parity

In override mode, traffic is restricted to one data byte to an RTU or one data byte from an RTU as follows

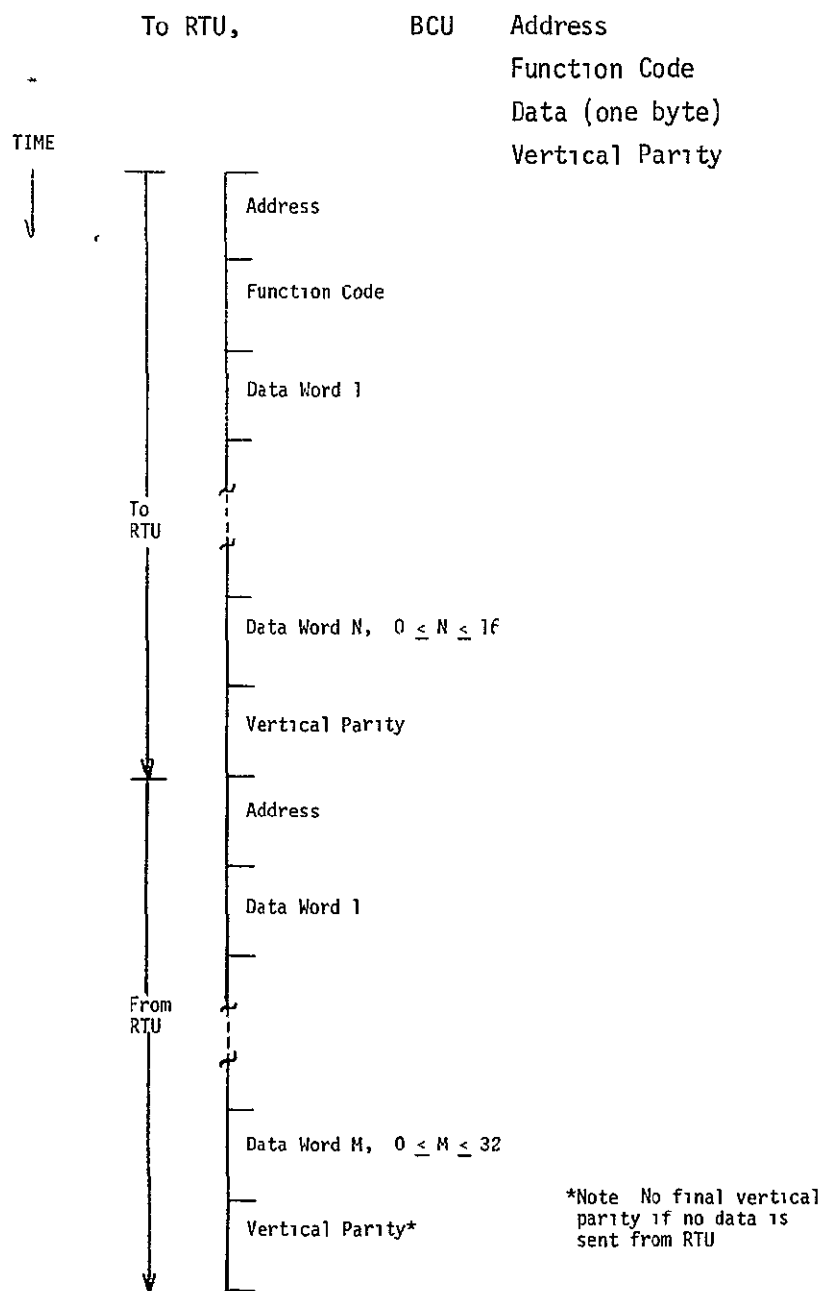


FIGURE 8-3 Standard Mode General Message Format

| | |
|-----------|-------------------|
| RTU | Address (its own) |
| From RTU, | BCU |
| | Address |
| | Function Code |
| | Vertical Parity |
| | RTU |
| | Address (its own) |
| | Data (one byte) |
| | Vertical Parity |

Control Logic and I/O

Figure 8-4 shows the RTU in somewhat more detailed block form, with special emphasis on the control logic. In operation, detection of the first message bit forces the RTU into the reset state. The first received byte (an RTU address) is compared with the address of the RTU, which is wired into the unit. If a positive comparison is made, the remainder of the message is processed.

The second byte is a function code. The RTU has a 16 bit x 64 word read-only memory. The message function code is the first address within the ROM where the RTU will find a sequence of processing instructions. The 16 bit memory word is divided into the following parts:

| | |
|----------------------|--------|
| Next memory address, | 6 bits |
| System status, | 4 bits |
| Channel address, | 6 bits |

Because a next memory address is generally found at a given location, the control is able to execute a relatively long sequence of instructions by jumping from location to location within memory, cued by a relatively small-dimensional function code. The system status part is used to control specific housekeeping functions such as parity checking, sending parity, sending acknowledgement, and flagging the end of a process sequence. The channel address specifies which of the user interface channels is to be updated with the currently received bus byte or be interrogated and results output to the bus. Note the memory sequencing is synchronous with the bus byte rate. Thus the RTU always knows where to put incoming data or from where to get outgoing data.

In addition to those functions described, the RTU control also contains the logic for generating and checking both horizontal and vertical parity. For an incoming message, a parity error is signified to the BCU by the RTU's failure to reply with its address. Further action is up to the central processor.

MOS RTU

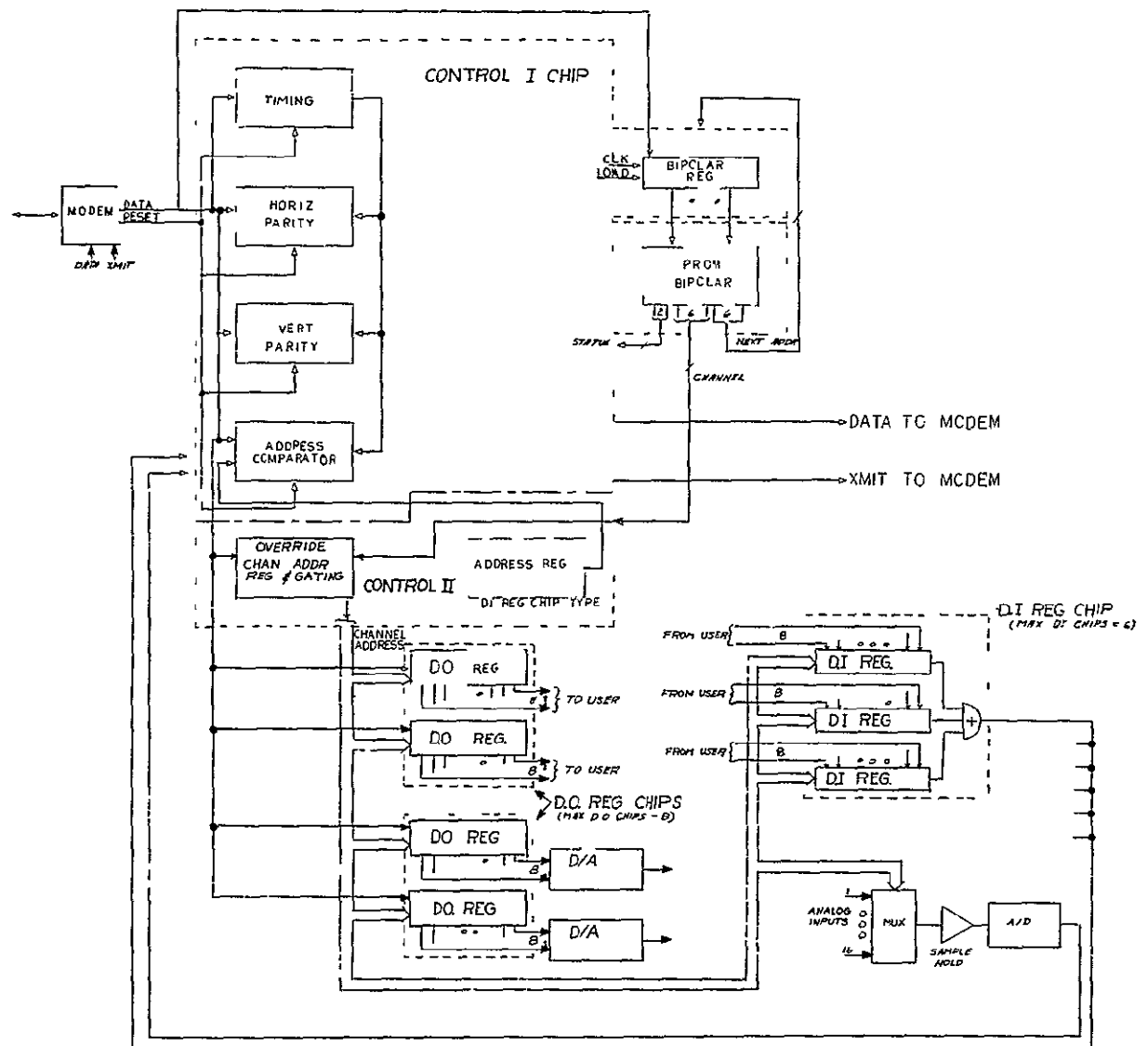


FIGURE 8-4 RTU Block Diagram

The RTU provides for fully buffered data transfer (analog or digital) at the user interface. The desired mix of inputs/outputs and analog/digital channels is configured into a particular RTU by combining standard modules. From zero to 16 RTU-to-user channels in any mix of analog or digital (8 bit words) can be accommodated. Any combination of 32 user-to-RTU channels in any mix are available. Digital interface can be in serial or parallel form. Digital to analog conversion (8 bit) is provided within the I/O section.

Chip Design

The RTU logic has been partitioned into four MOS/LSI chip types and one bipolar chip. The bipolar chip contains the memory address register, which has an extensive parallel interface with the bipolar ROM. Thus direct signal compatibility is assured.

The MOS/LSI chip types are as follows:

Control I bit counters, byte counters, parity checking and generation, miscellaneous gating and control. One per RTU.

Control II RTU address register, override address register, ROM control and switching.

Digital Output Two dual-rank registers with control for updating and serial shift-out.

Digital Input Three single-rank registers with control for updating and serial shift-out.

Figures 8-5, 8-6, 8-7, and 8-8 are logic schematics of these respective chips. Characteristics of the chips are summarized in Table 8-2.

TABLE 8-2 RTU Chip Characteristics

| | <u>Control I</u> | <u>Control II</u> | <u>Digital Output</u> | <u>Digital Input</u> |
|----------------------------|------------------|-------------------|-----------------------|----------------------|
| Input Pins | 11 | 22 | 17 | 39 |
| Output Pins | 10 | 13 | 16 | 1 |
| Number of Logic Cells | 107 | 47 | 92 | 75 |
| Number of Devices | 422 | 290 | 495 | 440 |
| Linear Mills of Cells | 440 | 294 | 530 | 402 |
| Estimated Chip Size (Mils) | 140 x 140 | 100 x 100 | 150 x 150 | 140 x 140 |

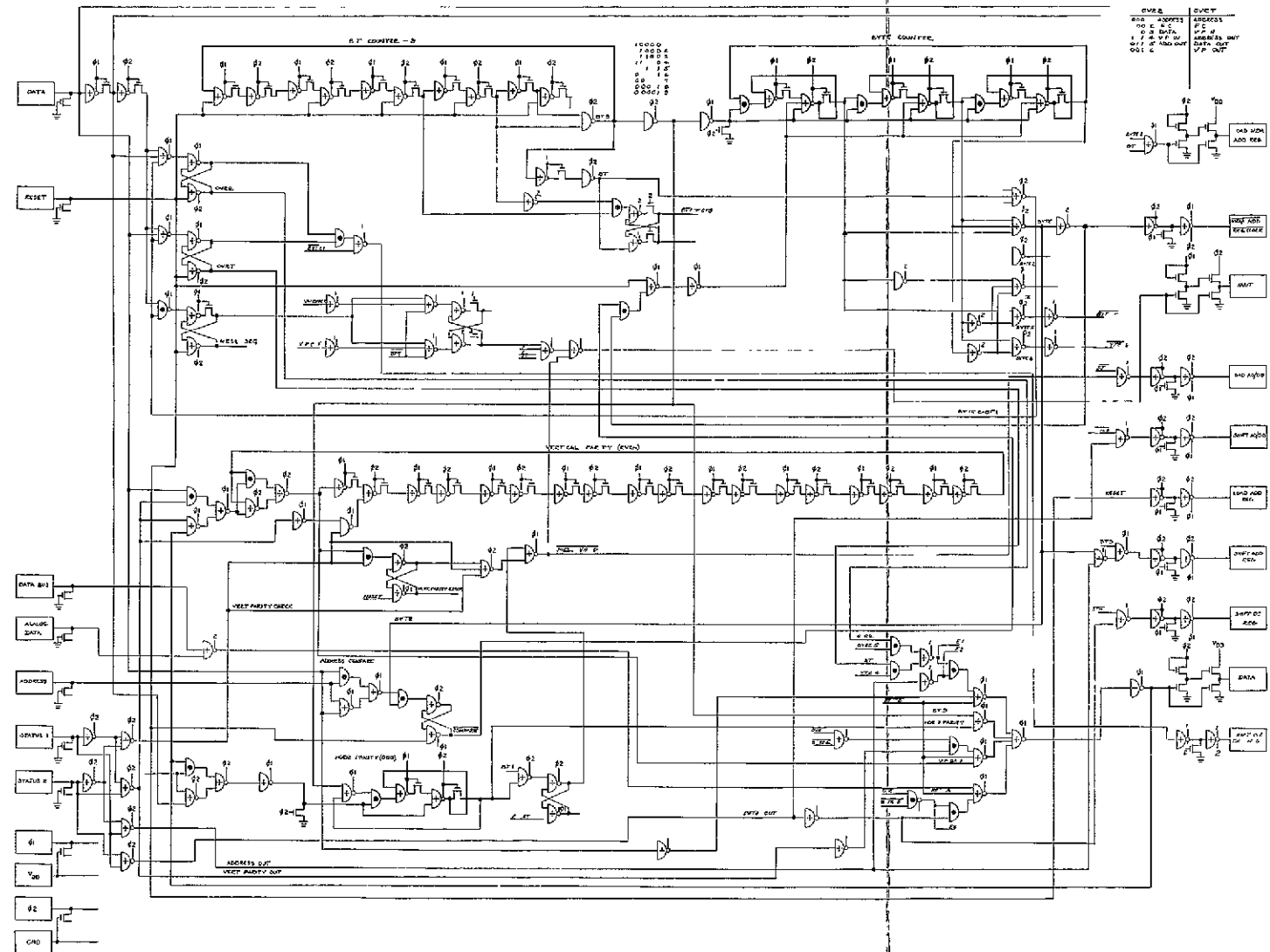


FIGURE 8-5 Logic Schematic, Control I Chip

This page intentionally left blank

FOLDOUT FRAME-2

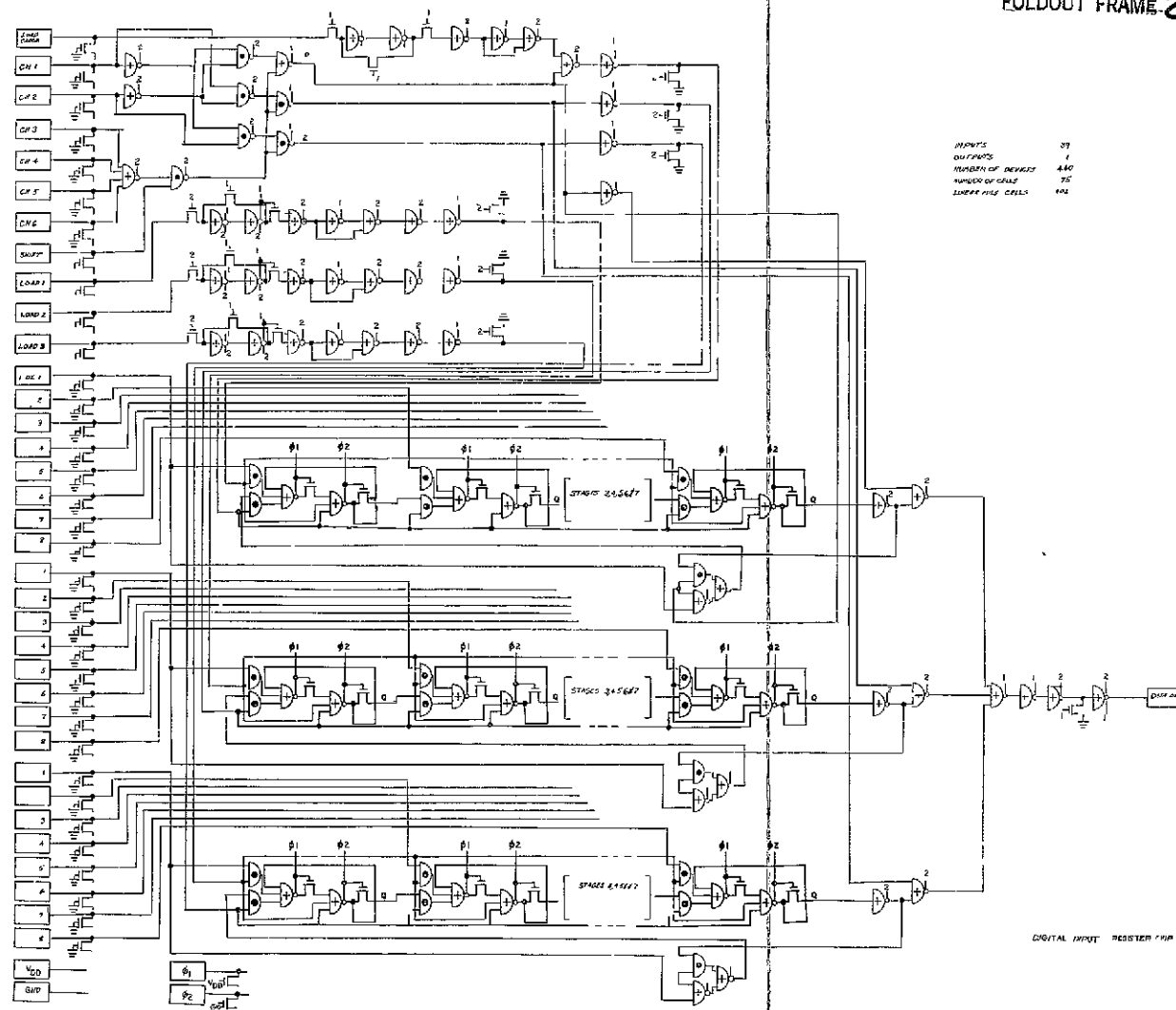


FIGURE 8-8 Logic Schematic, Digital Input Chip

9 0 ANTENNA GIMBAL ASSEMBLY

9 1 Function

The Antenna Gimbal Assembly (AGA) is a two axis drive assembly which controls the pointing of the antenna in response to motor drive signals from the Antenna Electronics Assembly (AEA). Each drive also provides accurate position data for antenna control. The gimbal axes, hereafter referred to as the inner and outer gimbals, are at right angles but non-intersecting. The antenna attaches to the inner gimbal which is carried by the outer gimbal. The outer gimbal mounts to the spacecraft mast. The angular range of the inner gimbal is ± 90 degrees and the outer gimbal is ± 110 degrees.

9 2 Configuration

Figure 9-1 shows the interface drawing of the Antenna Gimbal Assembly. The figure shows the gimbal axes relative to the spacecraft axes when the antenna is in the zero position. In this position, the inner gimbal is parallel to the spacecraft roll axis and the outer gimbal is parallel to the pitch axis. The stowed condition of the AGA for launch is shown in phantom. In this condition, the inner gimbal is constrained from rotating by an electro-explosive pin puller at the periphery of the drive. The outer gimbal is constrained from rotating by pinning the communication equipment compartment to the spacecraft mast.

Figure 9-2 shows the design layout of the Antenna Gimbal Assembly. Two identical drives are mounted together to form the two axis gimbal configuration. Each drive unit contains a stepper motor with integrally attached gearhead, a harmonic drive, dual speed resolver, and supporting bearings. A drive unit has the overall dimensions of 5 1/2 inch diameter by 7 inches long. Input power to each drive motor is 6.2 watts, maximum. The resolver power is 50 milliwatts. The assembly weight is approximately 15 pounds.

Each drive unit utilizes a 90 degree per step permanent magnet stepper motor as the prime mover. To meet the positioning, stability, and slew speed constraints, an output stepping resolution of 0.005 degree has been selected. Thus, an overall gear ratio of 18,000:1 is required. This is achieved by a gearhead of 149:1 ratio integral to the motor and a harmonic drive ratio of 121:1. For compactness, the motor/gearhead is contained inside the flexspline of the harmonic drive. The motor/gearhead and flexspline are fixed to and enclosed within the shaft. For

This page left intentionally blank.

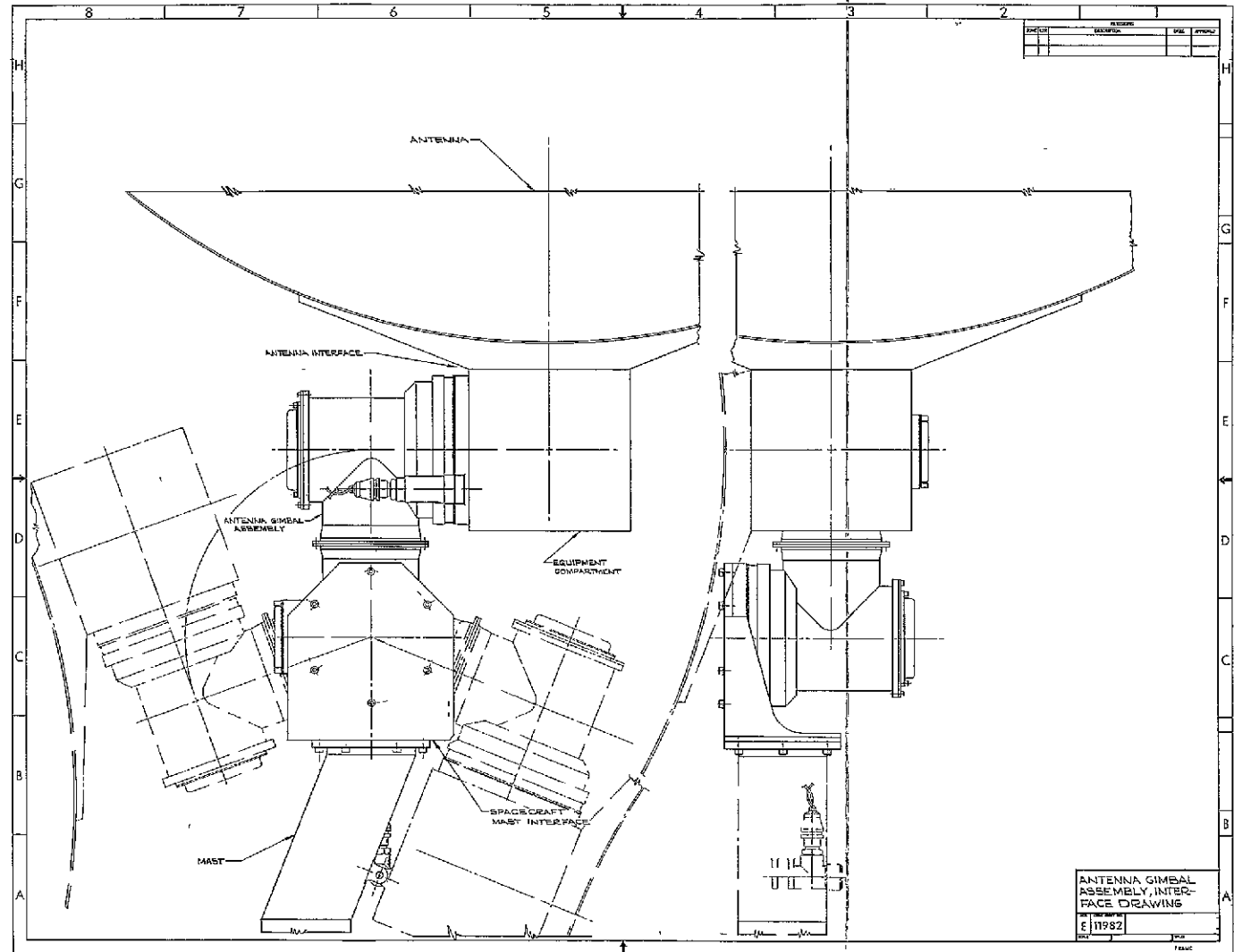


FIGURE 9-1 Antenna Gimbal Assembly Interface Drawing

This page left intentionally blank.

FOLDOUT FRAME 1

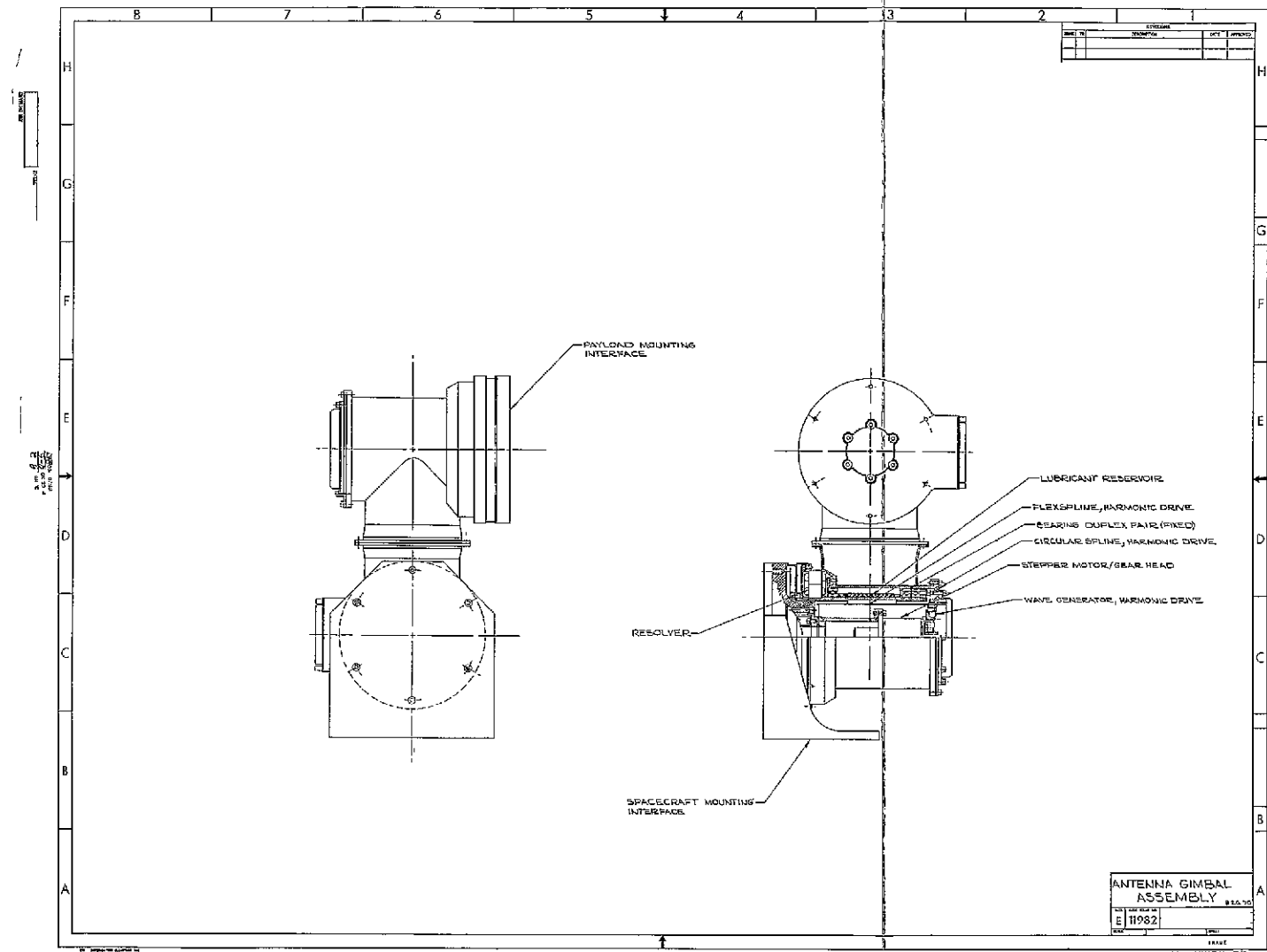


FIGURE 9-2. Antenna Gimbal Assembly Layout

This page left intentionally blank.

the outer gimbal, the flexspline is the fixed member and the circular spline, which is attached to the housing, is the rotating output member. For the inner gimbal drive, the circular spline is the fixed member and the flexspline is the rotating output member. The housing is supported on the shaft by a duplex pair of angular contact bearings at one end and a single angular contact bearing at the other end. The bearings were sized and spaced to resist the launch loads. The duplex pair is fixed to one end of the assembly, and the single bearing is fixed to the housing at the other end but allowed to float on the shaft to accommodate thermal expansion. The bearings are of 440C stainless steel with phenolic retainers and lubricated with NPT-4 oil. Nylasint reservoirs, impregnated with NPT-4 oil, are placed near or within all rotating, contacting components and lubrication is achieved by controlled leakage of lubricant vapor through non-contacting labyrinth seals. To provide position information, a dual speed resolver of pancake configuration is directly mounted to the shaft and housing. A coiled ribbon cable provides lead-in for the resolver secondary windings to allow angular freedom between stator and rotor with little restraint.

9.3 Operational Description

The Antenna Gimbal Assembly is inactive during all operations prior to PPCS turn-on. The assembly is stowed and caged for launch as described previously. Activation of the AGA does not occur until acquisition of the precision attitude reference. Activation is initiated by the firing of the electro-explosive pin pullers which release the gimbal drive units. The AGA is driven in response to AEA signals based upon targeting inputs. For PPCS operation in low altitude, sun-synchronous orbits, the AGA will point the antenna (either by command steer or auto-track) at one of three data-relay satellites in a geosynchronous orbit. As a function of visibility constraints the antenna must be retargeted from one satellite to another within 4 minutes, which establishes the slew requirement of the AGA. For PPCS operation in geosynchronous orbit, the antenna will be pointed continuously at a ground station, requiring very little AGA activity.

9.4 Performance Characteristics

Performance characteristics of the drive units are summarized in Table 9-1.

TABLE 9-1 AGA Drive Unit Parameters

| Parameters | Performance |
|---|---|
| Angular range | ± 90 degrees, inner gimbal ± 110 degrees, outer gimbal |
| Peak slew rate | 0.80 degree/sec |
| Stepping resolution | 0.005 degree/step |
| Overall gear ratio | 18,000:1 |
| Gear train efficiency (est.) | 70% |
| Running torque (slew speed) (tracking speed) | 12.0 ft-lb >12.0 ft-lb (dependent on speed) |
| Energized holding torque | >50.0 ft-lb |
| Unenergized holding torque (detent) | >5.0 ft-lb |
| Output spring rate (based on harmonic drive) | >4800 ft-lb/rad |
| Mechanical Error Sources | |
| • Backlash | Biased out by cable spring restraint |
| • Gimbal to antenna beam alignment | 0.8 min |
| • Bearing radial runout | 0.5 min. |
| • Thermal distortion | 0.6 min |

9.5 DESIGN

Motor

The stepper motor is a size 8, 90 degree per step, permanent magnet motor made by Kearfott. Two windings at a time will be sequentially energized to produce a running torque of 0.18 in-oz at 160 steps per second, equivalent to slew speed. The motor has been selected on the basis of carrying the reflected inertia load at the peak slew rate, with sufficient margin.

Specifications

| | |
|---------------------------------|--------------------------|
| Manufacturer | Kearfott |
| Part Number | CM4-019-007 |
| Type | Size 8, permanent magnet |
| Stepping angle | 90 degrees |
| Holding torque | 0.55 in-oz |
| Maximum stepping rate (no load) | 300 step/sec |
| Rotor inertia | 0.3 gm-cm ² |
| Input power (maximum) | 6.2 watts |
| Operating voltage | 28 v d c |

Gearhead

A gearhead with a ratio of 149:1 is integrally attached to the motor. At low stepping rates, as in tracking, the running torque of the stepper motor is 0.25 in-oz. Multiplying this value by the ratio of the gearhead, operating load torque of the gearhead is determined to be about 37 in-oz. A specially designed size 15 gearhead is specified to obtain high output torque capacity and to obtain the wear life required for an equivalent 300 million or more revolutions of the input pinion.

Specifications

| | |
|-----------------------|--------------------------------|
| Configuration | Bu Ord |
| Size | 15 or larger |
| Ratio | 149:1 |
| Operating load torque | >50 in-oz |
| Starting torque | <0.01 in-oz |
| Backlash | <30 arc minutes |
| Operating life | >300 million input revolutions |

Harmonic Drive

The output motion of the gearhead is reduced further by another stage of gear reduction. The harmonic drive was selected to obtain high reduction ratio and high torque capacity in a small package and to

obtain low backlash. The harmonic drive is identical to that used in the Project 777 Biaxial Drive Assembly, except for minor modifications in the circular spline configuration. The harmonic drive is specified by two TRW documents, Harmonic Drive Specification No. PT2-3073C and Source Control Drawing C256101. Some pertinent functional characteristics from the specification are given below.

Specifications

| | |
|----------------------|-------------------------|
| Gear ratio | 121:1 |
| Backlash | <0.5 arc minute |
| Static load capacity | >37.5 ft-lb |
| Spring rate | >4800 ft-lb/rad |
| Input inertia | <0.1 lb-in ² |
| Weight | <1.15 lbs |

Resolver

To provide high accuracy position information a dual speed resolver of pancake configuration is direct mounted on the shaft and housing. The sine and cosine outputs of the resolver are applied to an electronic encoding system which converts the resolver signals to digital angular information. The dual speed resolver consists of 32-speed sine and cosine windings for high accuracy information and single speed sine and cosine windings to resolve the position ambiguity of the multi-speed output.

Specifications

| | |
|--------------------------------------|--|
| Speeds | 32/1 Dual |
| Excitation | 8v (0-peak) 1024 Hz |
| Accuracy | 16 arc seconds (32-speed) 0.5 degree (1-speed) |
| Transformation ratio | 2.0 (32-speed) 0.4 (1-speed) |
| Input power | <75 milliwatts |
| Phase shift (over temperature range) | Rotor to stator $25 \pm 8^\circ$ Both speeds track within 0.5° |
| Weight | <1.0 pound |

Bearings

During launch the antenna/communication platform will be stowed and pinned to avoid backdriving of the AGA. Ball bearings of the torque tube variety were selected to meet the anticipated high loading and also for packaging convenience. The bearings were sized and spaced to resist the launch loads with sufficient margin. A duplexed pair of angular contact bearings is fixed at one end of the drive unit and a single angular contact bearing, which is allowed to float on the shaft, is used at the other end.

Specifications

| | |
|-------------------------------------|---|
| Type | Angular contact, face-to-face duplex pair |
| Bearing class | ABEC-7 |
| Bore | 3.0 inch |
| Outside diameter | 3.625 inches |
| Cross-section | 5/16 inch |
| Static load capacity (each bearing) | radial 2120 pounds thrust 6,100 pounds |
| Preload | 36 to 54 pounds |
| Material for balls and races | 440 C CRES |
| Material for retainer | phenolic |

10 0 ANTENNA ELECTRONICS ASSEMBLY

10 1 Function

The Antenna Electronics Assembly (AEA) provides the electrical interface between the Antenna Gimbal Assembly (AGA) and the Data Processing Subsystem. The AEA drives the AGA two-axis stepper motor gimbal drive in response to computer commands and encodes the gimbal angles using the multi-speed resolver signals.

10 2 Configuration

The AEA is packaged using the slice concept described in section 3.2. In this case there are 2 slices servicing 2 gimbal axes with resolver readout and motor excitation functions. The partitioning is as follows:

Encoder

Analog Encoder Board

Analog Encoder Board

Logic Board

Excitation and Motor Electronics

Common Electronics Board

Motor Electronics Board

The two analog encoder boards are identical and the motor electronics board has two identical halves. Table 10-1 lists physical characteristics of the AEA.

Table 10-1 Antenna Electronics Physical Characteristics

| | |
|---------------------|-------------------|
| Slices | 2 |
| Boards | 5 |
| Dimensions | 3.2"h x 8"w x 6"d |
| Power | 6 watts |
| Components | |
| Integrated Circuits | 134 |
| Discrete Components | 238 |

10 3 Operational Description

During launch and initial spacecraft orientation, the AEA is quiescent with no power applied. The antenna gimbal is pinned in place to survive launch loads. After the gimbal has been released, the AEA is turned on and drives the gimbal in response to a commanded rate from the computer. The servo loop is closed in the computer. No distinct operating modes are discernable to the electronics. The computer commands rates that orient the antenna toward a target data relay satellite. This target is tracked until it leaves the gimbal FOV at which time the gimbals are slewed to a new target. An auto-track signal from the antenna may be used for pointing - this signal is sent directly to the computer with no processing by the AEA.

10 4 Performance Characteristics

Motor Control

| | |
|---------------|-------------------------------|
| Maximum Rate | 200 steps/sec |
| Form | Gray code, 4 phase, switching |
| Maximum Power | 6.2 watts |

Resolver Encoding

| | |
|------------------------|--|
| Technique | Dual speed, double angle phase shift with zero crossing detectives |
| Excitation | 1.024 kHz, Sine |
| Resolution | 0.005° |
| Accuracy (Electronics) | 0.003° (1σ) |
| (Resolver) | 0.008° (1σ) |
| Range | ±110° |

10 5 Design

The Antenna Electronics Assembly provides the electronics required to operate the antenna gimbal in two axes, including position encoding and motor activation. Figure 10-1 is a block diagram. Position is sensed using dual-speed resolvers. The AEA excites the resolvers with a sinusoidal signal of frequency 1.024 kHz, and it encodes the resulting resolver output signals to digital position values. The control loop for positioning the antenna is closed through the

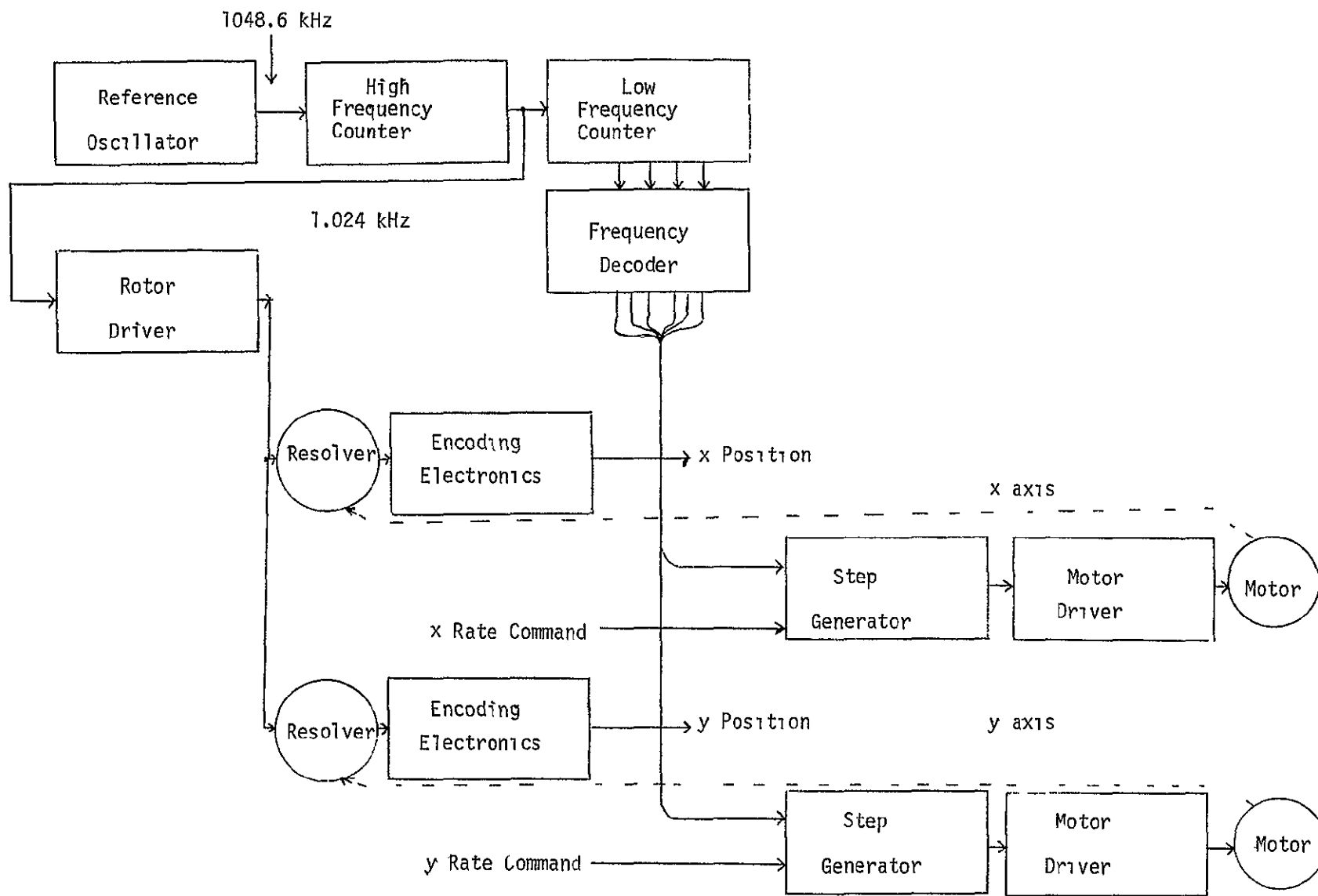


Figure 10-1. Antenna Electronics Assembly Block Diagram

spacecraft's central digital processor. The forward portion of this loop is mechanized as a digital rate device. Rate command comes from the computer in whole-word parameter form. This data is converted to a step rate within the AEA, and the gimbal motors, which are of the stepping type, are driven accordingly via the power drivers.

Resolver Encoding

Drawing X264494 (Figure 10-2) shows schematically that AEA circuitry which is common to both axes. The crystal-controlled reference oscillator generates a frequency of 1048.6 kHz in logic signal format. The frequency counter, composed of logic MSI elements, divides this frequency by stages to a final level of 1.6 Hz. Most of the intermediate levels are used, the chief ones from a conceptual point of view being 1.024 kHz and 204.8 Hz. The values from 1048.6 kHz through 1.024 kHz are used in the position encoders, while those from 204.8 Hz through 1.6 Hz are used in driving the motors.

The 1.024 kHz square wave is filtered of harmonics, power amplified, and applied to the resolver rotors. The result is a very pure sinusoidal excitation at that frequency.

The frequency decoder is a logic combinational circuit which produces an ensemble of pulse rates from 102.4 Hz to 1.6 Hz, having the property that no two lines have a pulse simultaneously. This signal set is used in each of the motor electronics sections.

Drawing x264495 (Figure 10-3) shows the resolver encoding circuitry for one axis. Each resolver has a single-speed section and a 32-speed section. Thus, two encoders are required. Consider first the single-speed section. The resolver is excited

$$V_e = V_m \sin \omega_e t$$

where V_m is the excitation peak amplitude, about 8 volts, and ω_e corresponds to 1.024 kHz. The stator output signals are

$$V_s = k V_m \sin \theta \sin (\omega_e t + \phi_r)$$

$$V_c = k V_m \cos \theta \sin (\omega_e t + \phi_r)$$

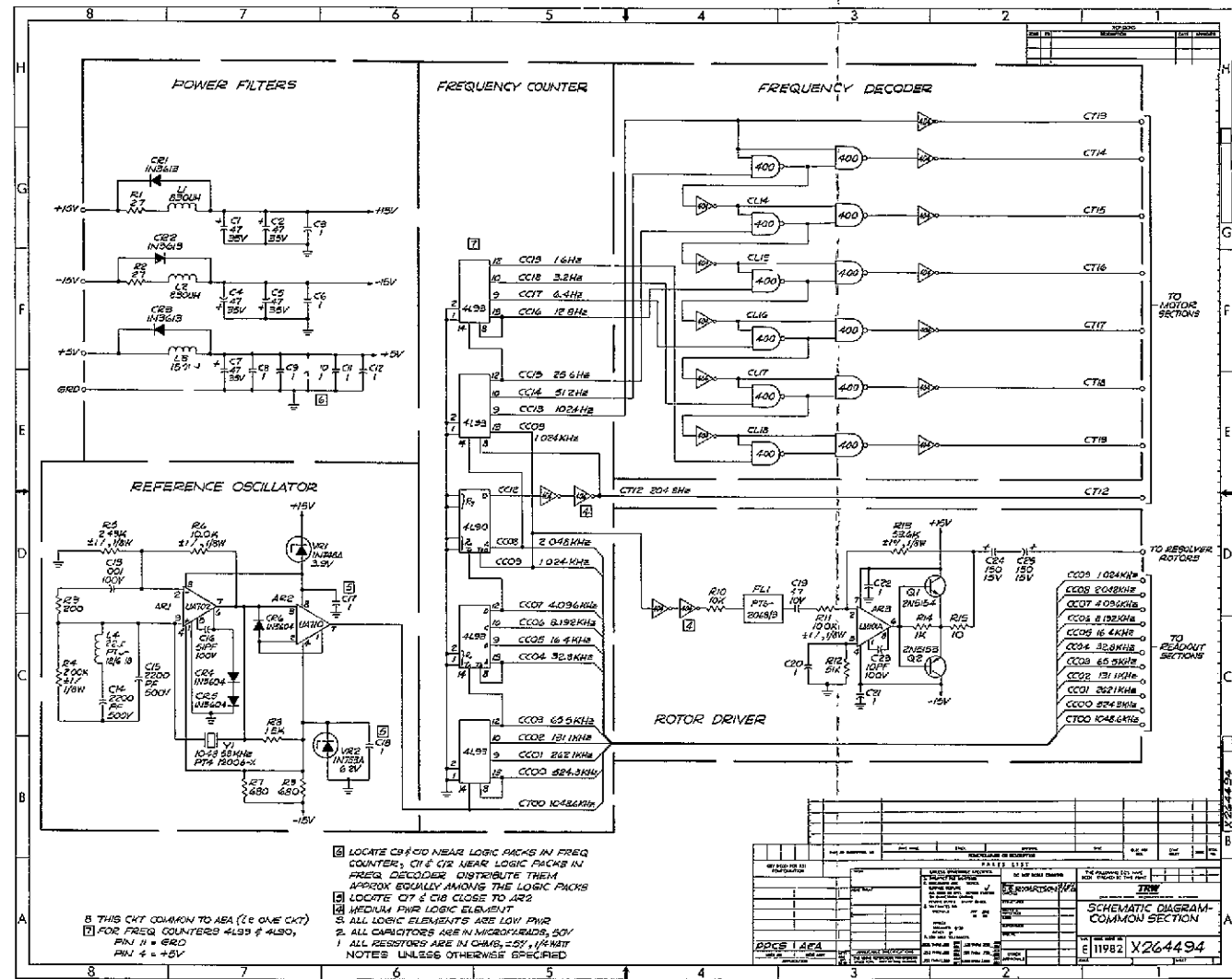


Figure 10.2 AEA Common Section

where k is a gain constant associated with the resolver winding ratio, and θ is the resolver's mechanical shaft angle. A phase shift ϕ_r , which is inherent to the resolver's electrical parameters, occurs from rotor to stator. These signals are squared and summed to yield a voltage which has the form

$$\begin{aligned} & \sin^2 \theta \sin^2 (\omega_e t + \phi_r) + \cos^2 \theta \sin^2 (\omega_e t + \phi_r) \\ &= (\sin^2 \theta + \cos^2 \theta) \sin^2 (\omega_e t + \phi_r) \\ &= \sin^2 (\omega_e t + \phi_r) = 1/2 [1 - \cos 2 (\omega_e t + \phi_r)] \end{aligned}$$

This signal is high-pass filtered to remove the DC component, zero-crossing detected, and frequency-divided by 2. The result is a phase reference signal of the same frequency as the resolver signals.

At the same time, the resolver signals are summed in such a manner that the sine signal is shifted in phase by -90° , resulting in a signal of the form

$$\begin{aligned} & kV_m \sin \theta \cos (\omega_e t + \phi_r) + kV_m \cos \theta \sin (\omega_e t + \phi_r) \\ &= kV_m \sin (\omega_e t + \phi_r + \theta) \end{aligned}$$

Note that this is a voltage whose phase, with respect to the developed reference, is equal to the shaft angle. It is zero-crossing detected to logic signal format.

The two logic phase signals are used to gate a 6 bit counter which counts at a rate of 65.5 kHz. Thus, at the end of a counting cycle the resolver angle has been digitized to one part in 64.

Encoding of the 32 speed resolver is somewhat similar in that a phase-shift technique is used, except that a "double-angle" pair of phase signals is produced. If we ignore the resolver phase shift, the combination of the resolver signals can be described

$$\begin{aligned} V_1 &= kV_m \sin 32 \theta \cos \omega_e t + kV_m \cos 32 \theta \sin \omega_e t \\ &= kV_m \sin (\omega_e t + 32 \theta) \\ V_2 &= kV_m \sin 32 \theta \cos \omega_e t - kV_m \cos 32 \theta \sin \omega_e t \\ &= kV_m \sin (\omega_e t - 32 \theta) \end{aligned}$$

11 0 Experiment Gimbal Assembly

11 1 Function

The Experiment Gimbal Assembly (EGA) provides 3-axis ground oriented pointing for large payloads in response to motor drive signals from the Experiment Electronics Assembly. Precision gimbal angle encoders are provided. By removing the middle gimbal axis, a two axis gimbal is derived which provides large angle rotation capability useful for space-oriented payloads.

11 2 Configuration

Schematic

A perspective schematic of the three-axis earth-pointing EGA geometry is shown in Figure 11-1. The unit attaches to the boom at one end of the X-axis and the payload, which is divided into two parts, is mounted at the ends of the Y-axis shaft. The X and Y axes are capable of ± 50 degrees of rotation. The Z-axis is capable of ± 15 degrees rotation.

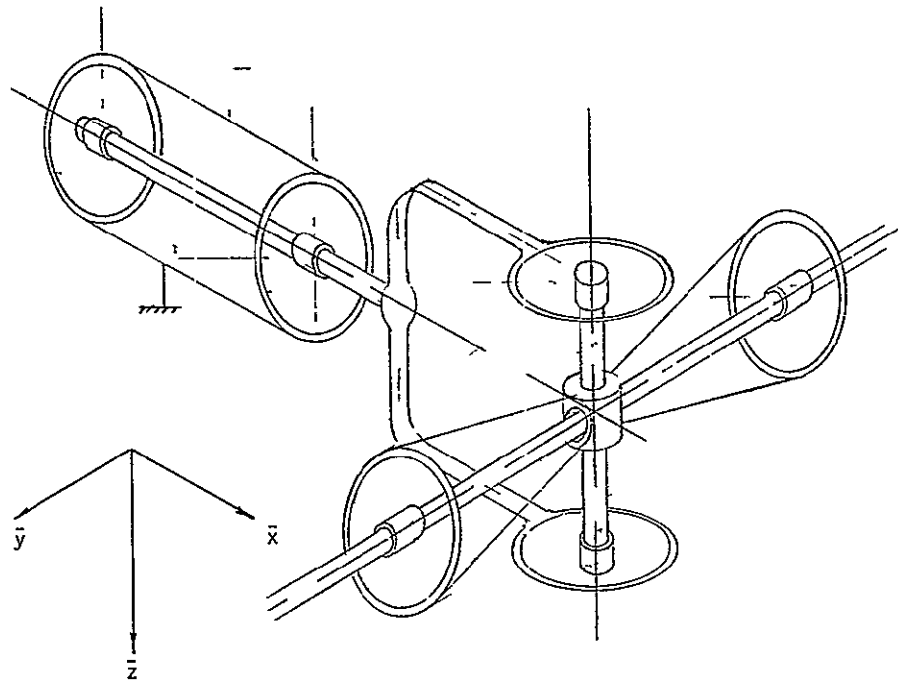


Figure 11-1 Earth Pointing EGA Configuration

The space pointing configuration of the EGA requires only two axes, each with full 360° rotation capability. This configuration is easily derived from the three-axis EGA by simply eliminating the Z-axis. Figure 11-2 is a schematic of the space pointing EGA. Note that the X-axis shaft is attached directly to the Y-axis housings.

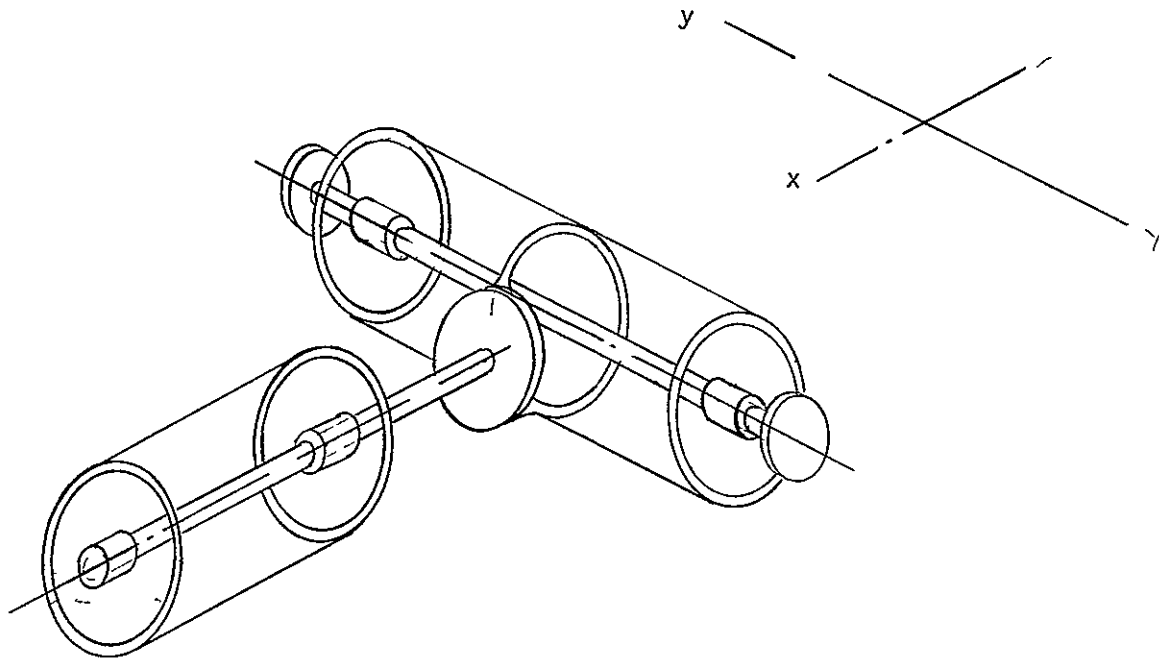


Figure 11-2 Space Pointing EGA Configuration

Layout

Figure 11-3 is a layout drawing of the unit. Each shaft is supported from its housing by means of flexures and ball bearings. The shafts and housings are connected as follows:

- The X-axis housing is bolted directly to the boom.
- The X-axis shaft and the Z-axis housings are rigidly attached to the gimbal ring.
- The Y-axis housings are rigidly attached to the Z-axis shaft by means of adapter fittings. The Z-axis shaft has a lateral opening in it which affords free passage for the Y-axis shaft.
- The payload is rigidly attached to the ends of the Y-axis shaft.

Each axis incorporates the following components:

- Angular contact ball bearings, nylon lubricant reservoirs and low clearance lubricant seals.
- Axial and radial bearing support flexures.
- Inductosyn plates for angular position measurement, associated axial flexures and preamplifiers.

Operational Usage

Operational command and control is provided in the Experiment Electronics Assembly. The basic operational modes are slewing and tracking. Performance characteristics of interest are

| | |
|---|---------------------------|
| Slew Rate | 3.0 deg/sec |
| Tracking Rate | 1.2 deg/sec |
| Acceleration to both Tracking and Slew | 0.10 deg/sec ² |

Under computer control, pointing modes including local vertical, local vertical offset, geographic track, and space track can be commanded. A calibration phase to remove large static errors is necessary to achieve the desired pointing accuracy.

11.4 Performance Characteristics

Gimbal freedom

| | |
|------------|----------------|
| Z-axis | $\pm 15^\circ$ |
| X & Y axis | $\pm 50^\circ$ |

| | |
|---|---------------------------------------|
| Tracking rate, each axis | 1.2 deg/sec |
| Slew rate, each axis | 3.0 deg/sec |
| Maximum angular acceleration, each axis | 0.10 deg/sec ² |
| Minimum torque available, each axis | 192 oz-in |
| Average torque required, each axis | 96 oz-in |
| Bearing friction torque, each axis | 10 oz-in running 15 oz-in breakout |

| <u>Total power consumption</u> | <u>Continuous</u> | <u>Peak</u> |
|---|--------------------------|---------------------------|
| Motors | 8.1 | 32.4 |
| Inductosyns | 20.0 | 20.0 |
| Heaters | * | 72.0 |
| Amplifiers | <u>1.8</u> 29.9 watts | <u>1.8</u> 126.2 watts |
| Power leads routed to payload (16 gauge wires) | | 8 |
| Signal leads routed to payload (28 gauge wire) | | 41 |
| Minimum structural stiffness | | 100,000 lb-ft/rad |

* Highly dependent upon orbit

Weight

| | |
|---------|------------|
| EGA | 100* |
| Payload | <u>540</u> |
| Total | 640 lbs |

Total mass unbalance (payload plus EGA) 0 2 lb-ft

Spacing between payload attachment flanges 28 00 in

Offset of the Y and Z axes from the boom attachment flange 26 30 in

Total length of the Z axis 27 00 in

Envelope diameter of each axis over the flexure supports 13 20 in

Accuracy

Repeatable Mechanical and Electrical Errors

Angular relationships of axes $\pm 0.5^\circ$

Launch vibration and shock induced change in angular relationships of axes $\pm 0.5^\circ$

Maximum shaft coning angle (bearings, 180° rotation) $\pm 0.9^\circ$

Alignment of inductosyns 1.5°

Basic inductosyn error $\pm 5.0^\circ$

Inductosyn error due to shaft coning $\pm 0.15^\circ$

Random Mechanical and Electrical Errors

Shaft coning angle (bearings, 180° rotation) $\pm 0.5^\circ$

Basic inductosyn error $\pm 0.3^\circ$

Inductosyn error due to shaft coning $\pm 0.09^\circ$

Stability Errors

Thermal Distortion

X-axis 1.5°

Y-axis 0.1°

Z-axis 0.2°

Associated Inductosyn Errors

X-axis 0.2°

Y-axis 0.02°

Z-axis 0.02°

* For 5Hz Natural Frequency to 75 lbs For a 2 Hz Natural Frequency, this can be reduced

11.5 Design

Refer to the layout drawing, Figure 11-3.

Bearings

Each shaft is supported by means of angular contact, ultra precision ball bearings. The outer races of the bearings are referenced to the housings by means of flexures which permit adjustment of the axial preload and perpendicularity of the shaft centerline of rotation with respect to the other axes. The inner races of the bearings are pressed onto the shafts and held axially by means of split ring retainers. In order to minimize runout of the shaft centerlines, the inner race grooves are ground after the inner races are pressed onto the shafts. The balls, ball separators and outer races are then assembled as part of the unit assembly sequence. Lubricant reservoirs are provided on the outer race of each bearing which consist of nylasint blocks impregnated with lubricant and supported by metal retainers. Holes are provided in the retainers at the outer race for short reservoir-ball access paths. Escape of the lubricant to space is minimized by means of low clearance seals at the ends of each housing. The lubricant selected for this application is Dupont Krytox[®] 143 AC per TRW Material Specification MT7-4-1. This type lubrication system has been successfully used by TRW Systems in several space qualified electro-mechanical components.

Bearing Specifications

| | |
|------------------------|---|
| Type | 15° Angular Contact |
| Class | ABEC 9 |
| Bore | 2.750 in |
| Outside Diameter | 4.500 in |
| Ball Diameter | .250 in |
| Preload | 150 lb |
| Race and Ball Material | 440 C Steel |
| Retainer Material | Phenolic - Porous |
| Manufacturer | Industrial Tectonics, Inc. (Custom Design) |

Bearing Flexure Supports

The ball bearings are supported by three-legged axial flexures and multiple beam radial isolation flexures. Figure 11-5 is a perspective drawing which illustrates the radial isolation flexure and the legs of the axial flexure. The radial beams provide uniform distribution of the preloads applied through the three axial legs. A total of 144 relatively flexible beams are used. The three-legged axial flexure provides bearing preload adjustment and allows thermally induced axial motion without angular errors being introduced.

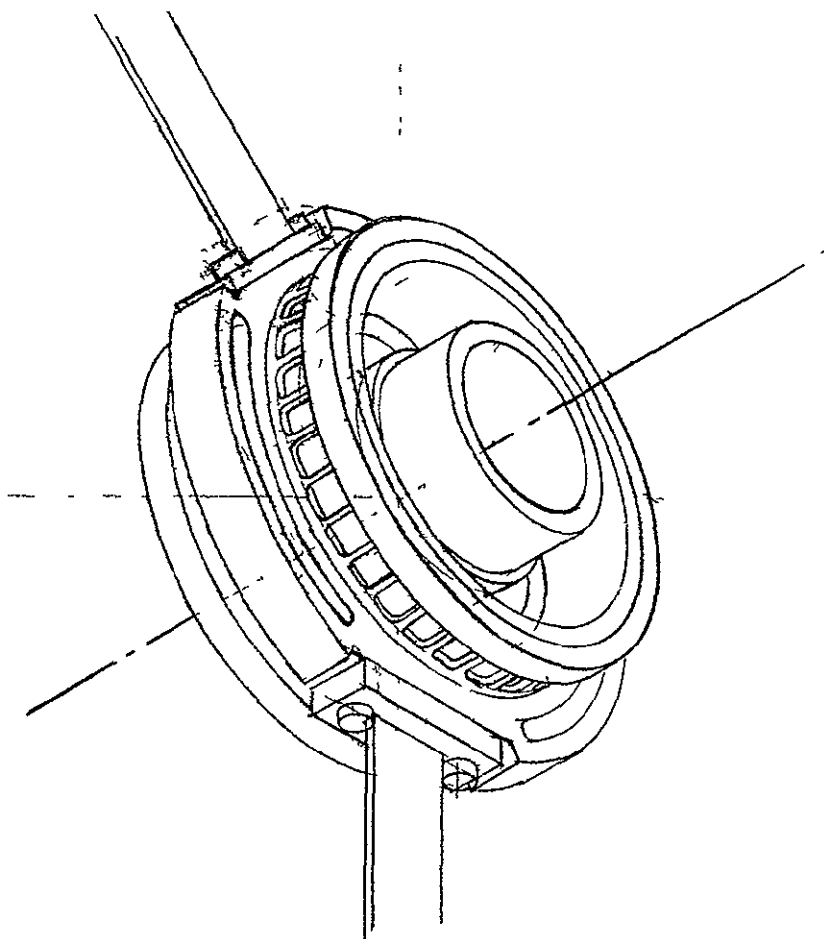


FIGURE 11-5 Isometric View of Radial Flexure

Inductosyn Plates

Rotary inductosyn plates are utilized for angular position measurements. The unit selected for this application has a 256 speed output which gives the desired accuracy and a single speed output which is necessary to avoid ambiguity. The inductosyns have been mounted at the ends of the shafts to provide access for performing precision adjustments. Because of the close spacing necessary between the plates, it is necessary to incorporate axial flexures to permit relative motion between the plates to exceed .005 inches. When the shaft moves to reduce spacing, a stop on the rotor mount contacts the stator mount which causes the stator to move off its stops, thus preventing further reduction of spacing. The flexures, which are attached to the stator mount, preload the stator against its stops and permit axial motion away from the rotor.

Inductosyn Specifications

| | |
|-------------------------------|-----------------------|
| Speeds | single and 256 speed |
| Accuracy - 256 speed | |
| Repeatable error | ± 3.0 sec |
| Non-repeatable error | 0.3 sec |
| Power | 4.0 watts |
| Nominal gap | 0.07 in |
| Nominal transformation ratios | |
| Single speed | 1.23×10^{-3} |
| 256 speed | $.65 \times 10^{-3}$ |
| Outside Diameter | 7.000 in |
| Inner Diameter | 3.375 in |
| Weight | 1.20 lb |
| Manufacturer | Farrand Controls, Inc |

Preamplifiers

Four preamplifiers, mounted in a single package, are necessary to amplify the output signals from the inductosyn prior to transmission to the spacecraft main body. These are located in close proximity with the inductosyns and connected with fully shielded lines.

Brushless DC Motors

The motors used are modified versions of the Star Tracker Gimbal motors produced by Shaeffer Magnetics, Inc. They are twelve-speed synchronous motors which are electrically commutated using the position signals from the inductosyn.

Motor Specifications

| | |
|------------------|---|
| Type | 12 speed synchronous, electronically commutated to provide DC motor characteristics |
| Voltage | 18 volts, max |
| Outside diameter | 5.00 in |
| Inside diameter | 3.00 in |
| Manufacturer | Shaeffer Magnetics, Inc |

| | <u>X-AXIS</u> | <u>Y & Z Axes</u> |
|--------------------------------|---------------|-----------------------|
| Stall torque | 192 oz-in | 96 oz-in |
| Resistance | 30 ohms | 30 ohms |
| Weight | 2.5 lb | 1.88 lb |
| Steady-state power dissipation | 2.70 watts | 2.00 watts |

Data Link Subassembly

The data links provide multiple electrical paths between the shafts and the housings while generating a minimum amount of friction and introducing minimum torsional restraint. The units used are identical with those used on the Star Tracker Gimbal Assembly (Figure 11-6) except for the mounting arrangement. Two links are used per axis. Each link contains four flat conductor strips which have loops between the inner and outer guide members producing low friction rollamatic action.

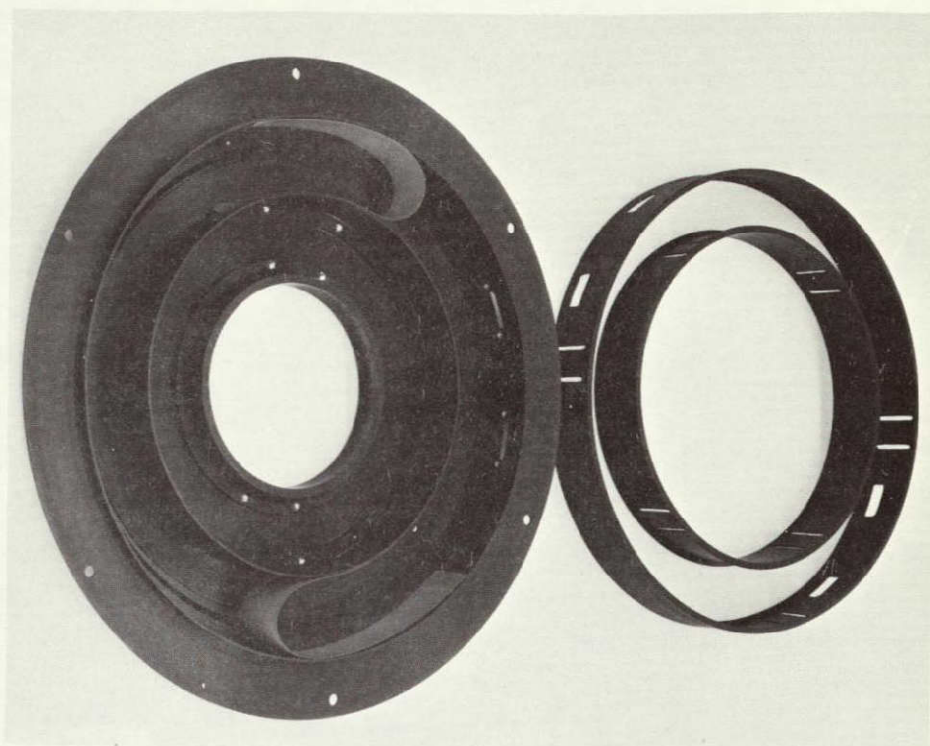


Figure 11-6. Data Link Assembly

Data Link Characteristics

| | |
|---|---------------------|
| Conductor strip manufacturer | Hughes Aircraft Co. |
| Part No. | H000855 |
| Number of strips per data link assembly | 4 |
| Number of conductors per strip | 11 |
| Total conductors per data line | 44 |
| Size of Conductor | .003 x .025 in |
| Spacing between conductors | .050 in |
| Insulation | |
| 1 layer FEP adhesive | .002 in |
| 2 layers Kapton Shield | .002 in |
| Spray capped silver epoxy | .001 in |
| Grounding | |
| Shield is grounded to any of the conductors at intervals of | 2.0 in |

Data Link Characteristics (Continued)

Insulation Resistance 75 volts/mil

Cross Coupling Noise

| (V _{in} = .5 V RMS) | <u>Freq-Hz</u> | <u>Volts-RMS</u> |
|------------------------------|----------------|-----------------------|
| | 10 KC | 5.5×10^{-6} |
| | 100 KC | 27.5×10^{-6} |
| | 1000 KC | 23.5×10^{-6} |

Caging

Preloaded stops are provided on the housing to limit the axial and radial motions of the shaft during launch vibration. The stops are loaded by means of bellville springs which serve to limit the maximum loads induced at resonant frequencies. Contact between the section of the stop on the shaft and that on the housing takes place at a 45° angle which makes the same set of stops effective both axially and radially. One of the stops is also used to limit the angular excursion to prevent contact of the Y-axis housing with the gimbal ring and to avoid damage to the wire wraps on the X and Z axes.

Thermal Control System

A schematic representation of the thermal control scheme is shown in Figure 11-6. All areas of the EGA, with the exception of narrow bands on the housings, are insulated with 20 layers of .25 mil aluminized Mylar sheet which forms a 1/4 inch layer. The exposed bands are radiating areas which reject excess heat. Heaters are bonded to the bands and controlled by means of thermistor sensors located in strategic areas. The Y and Z axis bands are painted white; the X axis, which is more significant thermally because of non-symmetry, is covered with secondary surface mirrors to minimize radiant heat input and resultant distortions. Critical sections will be controlled to a nominal temperature of 70°F. Heater power required to maintain this control will be highly dependent upon the orbit. A maximum of 72.0 watts is estimated for the worst case condition.

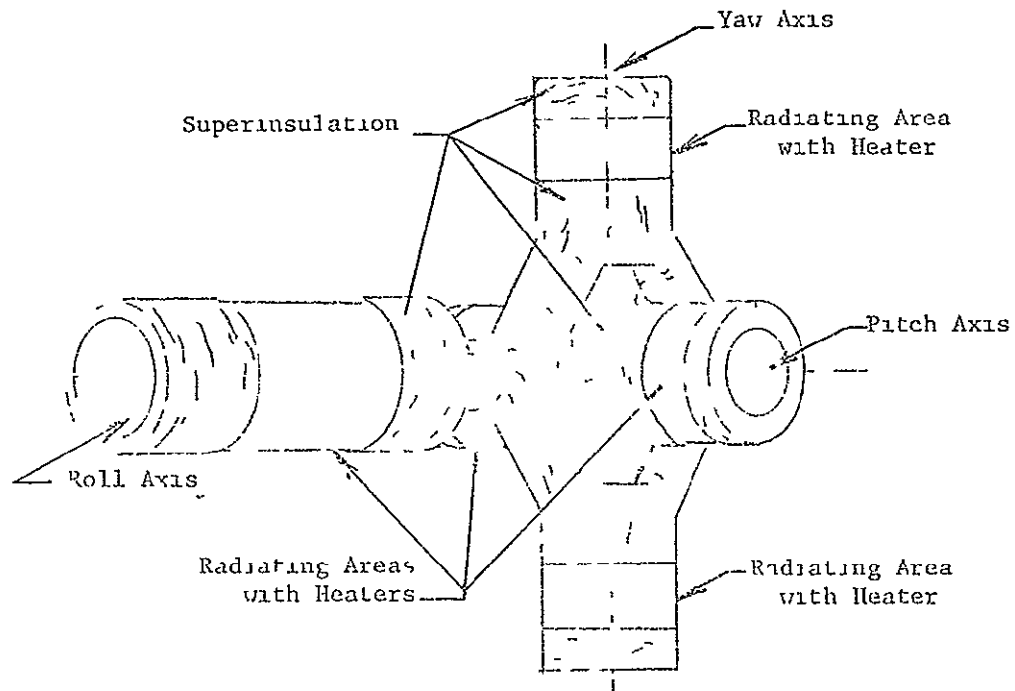


Figure 11-7 Thermal Control System

Test

A pair of air bearing pads are provided on each axis to relieve the ball bearings of 10 g loads during ground testing. The bearing friction which would be generated by these loads is far in excess of that which the servo system can tolerate for precision pointing. The pads shown on the layout drawing are designed for horizontal support of the axes. More precise ground testing can be accomplished with the axis under test supported vertically with a thrust type air bearing pad.

Materials

The following is a listing of the materials selected for principal EGA parts

| | |
|------------------------------|-----------|
| Shafts | Beryllium |
| Housings | Beryllium |
| Gimbal Ring | Beryllium |
| Y-axis shaft-housing adapter | Beryllium |
| Payload Attachment Flange | Beryllium |

| | |
|-------------------------------|---------------------|
| Bearing Isolation Flexures | 6A14V Titanium |
| Axial Flexures | 6A14V Titanium |
| Inductosyn Flexure | 6A14V Titanium |
| Radial Load Ring | 303 Stainless Steel |
| Wire Wraps | 2024 Aluminum |
| Motor Mounts | 2024 Aluminum |
| Removable Air Bearing Pads | 2024 Aluminum |
| Support Covers | 2024 Aluminum |
| Low Clearance Lubricant Seals | 2024 Aluminum |
| Lubricant Reservoirs | Nylasint |
| Ball Bearings | 440C Steel |

12 0 Experiment Electronics Assembly

12 1 Function

The Experiment Electronics Assembly (EEA) provides the electrical interface between the Experiment Gimbal Assembly (EGA) and the Data Processing Sub-system. The EEA encodes the EGA gimbal angles and controls and drives the gimbal motors.

12 2 Configuration

The Experiment Electronics Assembly is packaged using the "slice" concept, described in detail in Section 3.2. In this case there are 10 slices, servicing 3 axes with Inductosyn readout and motor electronics functions. The partitioning is as follows:

Excitation Slice

Excitation Board

Motor Electronics, X-axis

Preamp Board

Power Amp Board

Power Amp Board

Single-Speed Encoder, X-axis

Analog Board

Logic Board

Multi-Speed Encoder, X-axis

Analog Channel Board

Analog Channel Board

Logic Board

Motor Electronics, Y-axis

Preamp Board

Power Amp Board

Power Amp Board

Single-Speed Encoder, Y-axis

Analog Board

Logic Board

Multi-Speed Encoder, Y-axis

Analog Channel Board

Analog Channel Board

Logic Board

Motor Electronics, Z-axis

Preamp Board

Power Amp Board

Power Amp Board

Single-Speed Encoder, Z-axis

Analog Board

Logic Board

Multi-Speed Encoder, Z-axis

Analog Channel Board

Analog Channel Board

Logic Board

The axis sets, a set being composed of a Motor Electronics slice, a Single-Speed Encoder slice and a Multi-Speed Encoder slice, are identical. In addition, the Single-Speed and the Multi-Speed Encoders are identical to those used in the Sensor Electronics Assembly.

The completed assembly is similar in appearance to Figure 3-3, the Sensor Electronics Assembly, except that its overall width is 16 inches, because of the extra number of slices. Slices will be mounted side-by-side, not vertically.

Table 12-1 lists the physical characteristics of the Experiment Electronics Assembly.

TABLE 12-1 Experiment Electronics Assembly, Physical Characteristics

| | |
|------------|---------------------|
| Slices | 10 |
| Boards | 25 |
| Dimensions | 8" h x 16" w x 6" d |
| Weight | 11 lbs |
| Power | 20 watts quiescent |

12.3 Operational Description

The functions performed by the Experiment Electronics Assembly are largely the same as those performed by the Sensor Electronics Assembly. Indeed, much of the circuitry is identical. In this case, 3 axes of Inductosyn encoding are performed and 3 axes of gimbal motor control are provided.

The Inductosyns used are identical to those on the Star Tracker Gimbal. As to the motors, they are similar in type, but have a greater power rating. They are 24 pole (12-speed), quadrature phase, permanent magnet types.

The main route of servo loop closure is via the computer. Hence, in this case the motor electronics differs in some respects from that of the SEA. There is no A-D converter. There are no distinct driving modes recognizable within the EEA. The exact form of the servo compensation function mechanized within the preamplifier differs as appropriate to the load characteristics.

Since the motor is of the same type, the method of commutation is identical. Finally, because of the higher power level, the motor power amplifier has an extra power stage, but the basic amplifier design is otherwise very similar.

12.4 Performance Characteristics

Table 12-2 summarizes the major performance characteristics for the Experiment Electronics Assembly. The contributions to Inductosyn encoding accuracy listed in Table 3-3 are equally applicable here, since the encoding circuitry is the same.

TABLE 12-2 EEA Performance Summary

| | |
|---------------------------------------|--|
| Inductosyn Encoding | Dual speed, phaselock resolver format encoders Three axis |
| Excitation Frequency (Sample Rate) | 10.5 kHz |
| Phaselock loop bandwidth | 200 Hz nominal |
| Resolution | 0.23 arc sec |
| Accuracy | ± 0.6 arc sec (1σ) |
| Range | 180 degrees |
| Motor Control | Quadrature, 12-speed drive Electronic commutation Three axis |
| Maximum voltage | ± 18 volts per phase |
| Delivered power | 22 watts max per axis |

12.5 Design

For the function of encoding the Inductosyn angles of the Experimental Gimbal, the circuitry is identical to that of the Sensor Electronics Assembly. The discussion of Section 3.5 with respect to the encoding is therefore applicable. For the function of driving the motors, the major significant difference is in the motor power amplifiers, since a higher power motor must be accommodated.

Drawing X264497 (Figure 12-1) is the schematic for the EEA Motor Electronics. The means of motor commutation, including the sine/cosine logic and the commutators proper, is identical to that described in Section 3.5. The power amplifiers are heavier with respect to current capability, as

represented by the additional symmetrical common-collector stage, Q7 - Q8

The exact form of the servo compensation, represented by the rate amplifier and the preamplifier, is yet to be determined. Hence the circuitry shown, which is similar to that of the SEA, is at this time to be considered merely representational.

REFERENCES

- 1 Preliminary Technical Report, PPCS Functional Design Analysis, and Error Analysis, TRW Report No 13900-6002-R0-00, 25 May 1970
- 2 Preliminary Technical Report, Attitude Reference Simulation Development for PPCS, R L Farrenkopf, TRW Report No 13900-6003-R0-00, 25 June 1970
- 3 Preliminary Technical Report, Pointing Simulation Development for PPCS, R P Iwens, TRW Report No 13900-6004-R0-00, 25 June 1970
4. Intermediate Technical Report, PPCS Functional Design and Analysis, TRW Report No 13900-6007-R0-00, 25 August 1970
- 5 Intermediate Technical Report, PPCS Error Analysis, R P Iwens, TRW Report No 13900-6008-R0-00, 25 August 1970
- 6 Final Report, Attitude Transfer Subsystem for the Precision Pointing Control System, P W Collyer, December 1970
- 7 Final Technical, PPCS Functional Design, Analysis, and Error Analysis, TRW Report No 13900-6012-R0-00, July 1971